

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

SINGLE-CHIP SURFACE-MICROMACHINED ACCELEROMETER (page 3)

Pulsewidth modulator increases laser-printer resolution (page 10)

High-performance ICs in single-supply analog circuits (page 15)

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Editor's Notes

ARCHITECTURES

The term "architecture" is classically defined as the art and science of designing and erecting buildings. Over time, it has come to connote the design and construction of practically anything, from ocean liners to written works, such as novels. In electronics, the term has come to mean the arrangement and interconnection of the building blocks of computers and other circuits. The term encompasses both individual efforts (the Pantheon, the Pentagon, the Pentium) and classes of designs (houseboat, honeycomb, Harvard architecture).




In this issue we describe some new ICs with interesting circuit architectures—for example, an electronic circuit that involves tiny physical edifices; our cover story describes the complete-on-a-chip ADXL50 micromachined accelerometer circuit, which is designed with an eye to properties in both the electrical and mechanical realms. In the systems arena, we mention (p.23) a *personal sound architecture* (PSA).

Or consider the AD830 (page 8), a feedback amplifier with two additive differential inputs, termed officially a "high-speed video difference amplifier", because of its applicability as a video line receiver. However, its designer, Barrie Gilbert, points out that that name—based on one major application—may cause us to miss the boat for many other applications, because it doesn't suggest that the device has a new and unusual architecture. He points out that it could just as well be called a video *summing* amplifier, because it will take sums as well as differences.


More fundamentally, however, it could be called a *voltage-balancing amplifier*, since, with appropriate feedback, it implements the equation,

$$V_{X1} - V_{X2} = V_{Y2} - V_{Y1}$$

Well, that's the kind of name that might induce yawns among casual browsers through our catalog. The name that Barrie believes to be precisely right for this type of architecture is *active feedback amplifier*, because it achieves its function through the use of voltage feedback via an active voltage-to-current-converter stage; in so doing, it provides high-impedance differential signal-handling at both the input and feedback ports. We've tried to hint at this in our headline, which—with a twinkle—calls it an "uncommon-mode high-speed video feedback amplifier with a difference." Will Barrie ever forgive us?

Finally, we close with the architectural prediction that a future issue will feature a monolithic 3-volt fast floating-point processor bearing the toothy new class designation of SHARC: Super-Harvard-ARchitecture Computer. 

CORRECTION

The AD817 and AD818 op amps (*Analog Dialogue* 27-1, page 19) were designed at our Wilmington MA semiconductor facility by Moshe Gerstenhaber and Alex Gusinov. Michael Gianino was the product engineer. 

Dan Sheingold

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(More authors on page 34)

Cover: The cover illustration was designed and executed by Shelley Miles, of *Design Encounters*, Hingham MA.

Analog Dialogue

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A Surface-Micromachined, Monolithic Accelerometer

ADXL50 : the first commercially available surface-micromachined device.

All signal-conditioning circuitry is on-chip

by Bill Riedel

The ADXL50* is a complete acceleration measurement system on a single monolithic chip. It's based on a differential capacitive, surface-micromachined polysilicon accelerometer integrated with signal conditioning circuitry, including a TTL-compatible self-test feature. The ADXL50 measures accelerations from 0 g to ± 50 g with bandwidth from dc to 1 kHz, producing an output voltage proportional to the acceleration. This makes it the first commercially available monolithic device to successfully incorporate traditional electronic semiconductor circuits with micromachined structures.

The ADXL50 is fabricated on Analog Devices' conventional BiCMOS production line which has been used extensively in the company's high-performance mixed-signal products. A surface-micromachining process produces tiny, highly complex mechanical structures from silicon (see sidebar on page 5, "Silicon that moves"). Since it uses many of the processing steps ordinarily used to manufacture traditional linear circuits, surface-micromachining lends itself readily to producing devices which combine both micromachined (mechanical) and semiconductor (electronic) elements on the same die. The ADXL50, exploiting this attribute, includes all necessary signal-conditioning, excitation, and test circuitry. Three external capacitors and a +5-volt regulated power supply are all that is required to measure accelerations to ± 50 g.

The micromachined sensor behaves electrically like a variable differential capacitor operating in a force-balance electronic control loop. The result is a measuring system that, unlike piezoresistive micromachined devices, is inherently stable over wide temperature ranges and—because it balances electrostatic force against acceleration force—is relatively independent of the mechanical properties of silicon. This force-balanced design also produces a very linear response due to the resulting minimal physical excursion of the beam during a broad range of acceleration values; typical nonlinearity is $< 0.2\%$.

A unique capability of the ADXL50 is a digitally activated self-test function which allows the sensor beam to be electrostatically deflected at any time to verify the integrity of the sensor element. This tests its ability to respond to an acceleration force (and provide a warning in case of malfunction)—a "must" in applications such as airbag systems in automobiles.

MEASURING ACCELERATION

Conventional techniques for detecting and measuring acceleration are all founded on principles first discovered by Newton and



outlined in his *Principia* in 1687. Newton's classical view holds that acceleration of a constant mass implies a force ($F = ma$, where F is force, a is acceleration, and m is mass). Most accelerometers operate by detecting the restoring force exerted on a mass by an elastic restraint.

Consider a simple mechanical system consisting of fixed mass, m , attached to a spring with stiffness, k . If the mass is displaced a distance, x , due to acceleration, the restoring force of the spring is $F = kx$. Substituting into Newton's equation, we find that $a = kx/m$ and can derive the magnitude of the acceleration by observing the displacement, x , of the restrained mass. This fundamental principle is used by even the most sophisticated and expensive electromechanical accelerometers; it is also how the micromachined ADXL50 works.

SENSOR MECHANISM

Figure 1 shows the layout of the ADXL50 chip. The heart of the chip is the surface-micromachined sensor located at the center of the die (Figure 2). Measuring only $500 \mu\text{m} \times 625 \mu\text{m}$ (less than $1/2 \text{ mm}^2$), the ADXL50 sensor resembles the letter "H" when viewed from above. The long, thin legs of the "H" are tethers that anchor the micromachined element to the substrate; they are the only electrical and mechanical contact between the sensor structure and the rest of the chip. The tethers form the spring system

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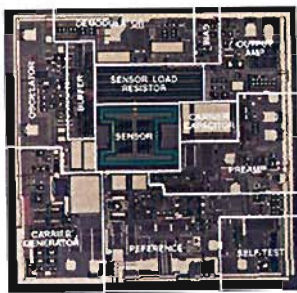


Figure 1. Layout scheme of the ADXL50 chip.

that suspends the central *test* (or *proof*) mass (the crossbar of the “H”) in tension within a well in the substrate; the mass is free to move in a direction perpendicular to the rethers (along the axis of the “H” crossbar), in the same plane as the substrate surface. When the device is packaged in a TO-100 metal can, the package tab is aligned with the “H” crossbar, showing the direction of sensitivity (see photo on page 3).

Projecting from the central proof mass is a series of regularly spaced filaments resembling the fingers of a comb (Figure 2). Each of these filaments is actually one plate of a series of parallel-plate variable capacitors; the other plates are attached to the chip substrate and interdigitate with the plates attached to the freely moving proof mass. Altogether, 42 moving capacitor plates [interdigitated with the fixed plates], attached to the sensor proof mass, are connected in parallel electrically for a total capacitance of only 0.1 pF. The plates anchored to the moving mass form the central plate of a three-plate differential capacitor structure. The plates anchored to the substrate and interdigitated with the moving plates are alternately connected in parallel; the effect is of two capacitors sharing a common plate, with capacitances of $Cx_0/(x_0 + x)$ and $Cx_0/(x_0 - x)$, where x_0 is the center position and x is the deflection caused by the acceleration (Figure 3).

Conceptually, the force exerted on the central proof mass by acceleration or deceleration in the direction of sensitivity causes it to move against the spring force of the tethers. This changes the relative spacing between the moving and fixed capacitor plates. The motion causes a fractional increase of capacitance on one side and a corresponding decrease on the other. The relative change in capacitance is proportional to the magnitude of acceleration, so acceleration can be determined by continually monitoring the electrical effects of capacitance changes.

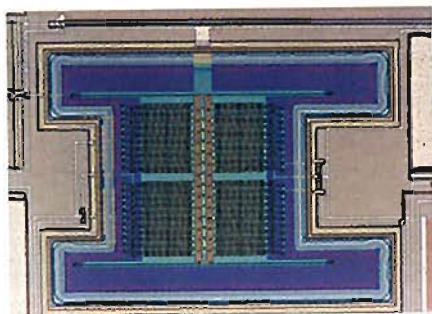


Figure 2. The acceleration sensor. Acceleration axis is vertical.

In actuality, the sensor operates within a force-balance electronic control loop; the proof mass, when accelerated, is restrained from moving (i.e., nulled, in the same manner as the summing point of an inverting operational amplifier) by the application of an opposing electrostatic force, generated by applying an inverted

version of the output voltage to the capacitor plates. This feedback produces a system which behaves essentially like one with a much stiffer spring constant (less nonlinearity and good temperature stability).

The physical shape and layout of the ADXL50's capacitive sensor fulfills a requirement for simplicity. The sensor is formed from a single layer of polycrystalline silicon. Since capacitor density (the number of elements with a given capacitance that can be placed within an area) is proportional to $1/d$, where d is the width and spacing of the plates, this feature is patterned using extremely fine lithographic fabrication and etching tools. Careful consideration of stresses in the polysilicon which forms the sensor allows these small structures to remain essentially level when suspended freely above the substrate. The sensor tethers—the finest structures—measure about $2 \mu\text{m}$ on a side and are about $200 \mu\text{m}$ long. The total physical mass of the measurement beam (proof mass) is less than 0.1 microgram. At rest, the spacing between adjacent capacitor plates is less than $2 \mu\text{m}$.

At these dimensions, silicon is highly elastic, easily withstanding shock and vibration—making it an ideal material for constructing finely patterned mechanical structures. In fact, on this scale, silicon has mechanical properties similar to those exhibited by steel at larger dimensions. As a result, the ADXL50's sensor is able to withstand physical shocks of 2000 g in any direction without suffering damage or deterioration in performance.

CIRCUIT TECHNOLOGY

The complete chip measures approximately 9 mm^2 and is dominated by the signal-conditioning circuitry, which surrounds the centrally located ($< 1\text{-mm}^2$) sensor. The circuitry includes a push-pull oscillator, carrier generator, reference, preamplifier, self-test circuit and an uncommitted output amplifier—providing a high level of system integration (Figure 4*).

The sensor, described earlier, consists of a pair of differentially varying capacitors that respond to the displacement of the mass. Square waves, V_A and V_C , at 1 MHz—of equal amplitude but 180° out of phase with one another—are applied to opposite plates of the capacitor pairs. Within each pair of plates, one side is biased to 3.4 V, the other to 0.2 V. The voltage at the proof mass, their electrical node, represents the degree of unbalance. At 0 g of acceleration, the central, moving set of capacitor plates is equidistant from each of the substrate-connected outer plates; their capacitances are equal, and—as a result—the two antiphase signals are equally coupled to the central plate and cancel each other, producing a nominal output voltage of 1.8 V (the midpoint of the 0.2-V and 3.4-V biased plates).

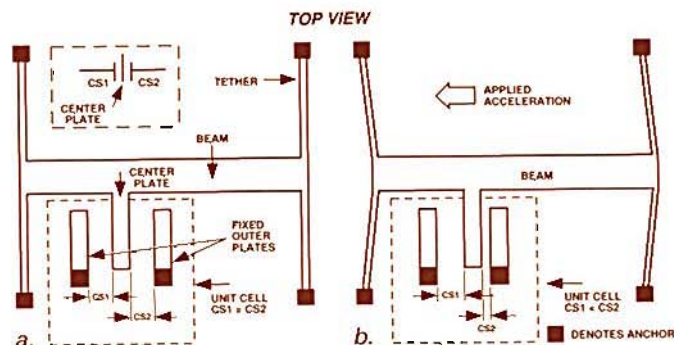


Figure 3. Simplified detail of the acceleration sensor showing one element of the differential capacitor.

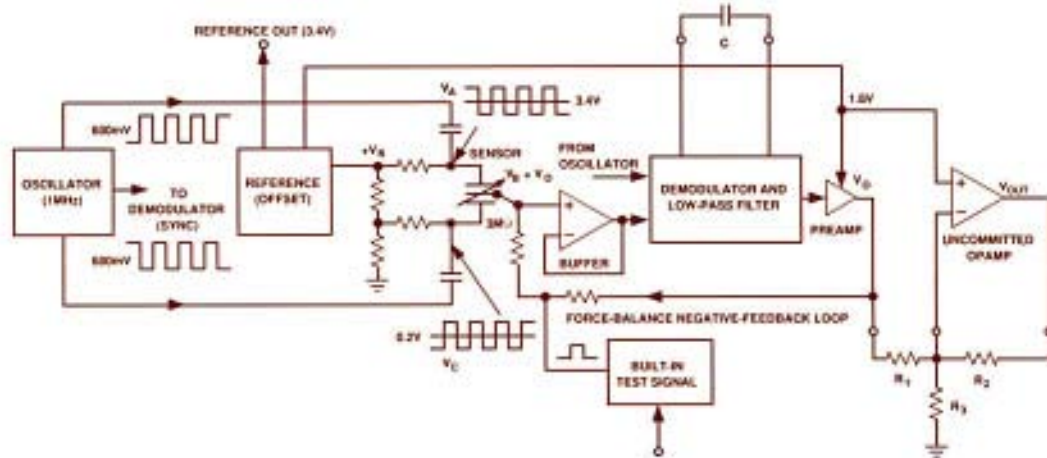


Figure 4. Simplified circuit details, showing the signal-conditioning circuitry and force-balance feedback loop of the ADXL50.

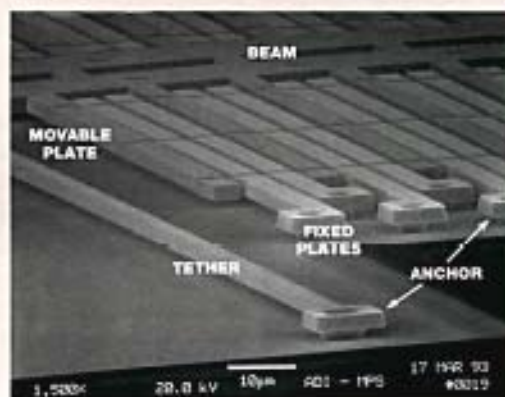
SILICON THAT MOVES

Micromachining is a processing technique used to manufacture tiny mechanical structures from silicon. A silicon wafer of the type used to make semiconductors can be etched (or modified) to produce small beams, masses, gears, and other structures measuring only a few thousandths of an inch.

Micromachining comes in two varieties: *surface* and *bulk*. Prior to the ADXL50, all the available micromachined devices used bulk micromachining. It was discovered in the 1950s that acid solutions attack different planes of crystalline silicon at different rates, depending on the crystal orientation. By exposing an area of silicon with a specific crystalline structure to acid, cavities with precisely angled walls are created.

Bulk micromachined accelerometers have existed for several years. Typically they consist of a membrane or diaphragm of silicon, roughly 10 μm thick, that is vertically formed in the wafer by chemical etching. In the center of the membrane is a large mass of silicon. On the top surface of the device, near the edge of the membrane, thin-film piezo-resistors sensitive to strain and deformation are deposited. Most of the membrane is removed, leaving tethers with these resistors suspending the central mass. Vertical acceleration causes the test mass to move, deforming the diaphragm and changing the resistance of the piezo-resistors. Bulk micromachined devices are large by IC standards—about 20× the size of the surface-micromachined ADXL50. Large size, coupled with the fact that the process for manufacturing bulk micromachines is inconsistent with semiconductor-circuit fabrication techniques, requires that signal-conditioning be off-chip. Bulk-piezo-resistive accelerometers are very sensitive to temperature effects and difficult to test fully.

Surface micromachining, a more sophisticated technique than bulk micromachining, creates much smaller, more-intricate and precisely patterned structures. It adapts manufacturing techniques perfected for making ICs to produce mechanical structures close to the surface of the silicon substrate. Chemical machining is accomplished by depositing, then etching, multiple thin films and layers of silicon and silicon-oxide to form complex mechanical structures. The feature dimensions of surface micromachined devices are typically 1 to 2 μm, similar to the feature dimensions of conventional electronic circuits. Most importantly, surface micromachining lends itself to the inclusion of conventional electronic circuitry on the same die. Thus, the surface-micromachined ADXL50 includes signal conditioning, resulting in a fully scaled, -referenced and -temperature-compensated volt-level output. Surface-micromachining leverages the cost economies of standard IC wafer-processing techniques, producing a highly integrated product at low cost.



input of a phase-sensitive demodulator, which is synchronized with the 1-MHz carrier; it rectifies and low-pass filters the signal. The single-pole filter's cutoff frequency is established by a single external capacitor; for example, 25 nF for 1 kHz.

The synchronous demodulator drives a preamp, which is referenced to +1.8 volts. The output of the preamp is fed back to the sensor through a 3-MΩ isolation resistor. This feedback voltage, applied to the sensor plates as a bias, causes an electrostatic restoring force to oppose the sensor's motion. In effect, the force-balance control loop acts to keep the sensor from moving, holding it close to its at-rest position. The correction voltage required to hold the sensor's proof mass (or central plate)

When the sensor experiences acceleration along the axis of sensitivity, the separations between adjacent plates will become unequal; one capacitance will increase while the other decreases. The 0.1-pF total capacitance generated between the beams changes by ±0.01 pF for ±50-g accelerations. The sensor structure can actually resolve as small a change as 20 attofarads (20 × 10⁻¹⁸ F), corresponding to a beam displacement of 0.2 Å. This resolution is a consequence of the precision of the associated signal-conditioning circuitry.

The output from the sensor array is a biased high-impedance square wave, V_B. This output is buffered and presented to the

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in the 0-g position is a direct measure of the applied acceleration. This voltage is available to the user at the output of the preamp.

The ADXL50 chip also contains an uncommitted op amp. Without further conditioning, the output of the single-supply ADXL50's preamplifier is 1.8 V at 0-g acceleration, with a span of approximately ± 1 V for a ± 50 -g acceleration range (i.e., 19 mV/g). The uncommitted op amp can be used to alter the 0-g voltage and/or amplify and filter the acceleration signal. In Figure 4, the noninverting input of the op amp is connected to +1.8-V signal, derived from an internal precision +3.4-V reference source. The scaling factor in the diagram is given by the ratio, $-R_2/R_1$, (since the amplifier is in inverting mode). For independent adjustment, gain is adjusted with R_1 and offset is adjusted with R_3 . Therefore, if the span desired is ± 2.25 V for the complete ± 50 g range, R_2/R_1 should be chosen such that:

$$\frac{R_2}{R_1} = \frac{V_{o_span}}{V_{pr_span}} = \frac{2.25}{1.0}$$

where V_{pr_span} is the output from the preamplifier and V_{o_span} is the desired span of the uncommitted amplifier output. Thus:

$$R_2 = 2.25 \times R_1$$

R_3 can be found from the following standard equation:

$$R_3 = 1.8 \text{ V} \frac{R_2}{V_{o0} - 1.8 \text{ V}}$$

where V_{o0} is the 0-g output level. Stated otherwise,

$$V_{o0} = 1.8 \text{ V} \left(1 + \frac{R_2}{R_3} \right)$$

With $R_1 = 100 \text{ k}\Omega$, $R_2 = 225 \text{ k}\Omega$, and $R_3 = 579 \text{ k}\Omega$, the output analog signal range will be +0.25 to +4.75 V for ± 50 g, with +2.5 V at 0 g. With 25 nF, the output signal's -3-dB bandwidth is 1 kHz, using the single-pole, 1-kHz filtering of the preamp. More-sophisticated configurations can provide multi-pole filtering without the use of additional active components.

SELF-TEST

Another unique attribute of the ADXL50 that sets it apart from alternative designs is the inherent ability to self-test the sensor and all associated on-chip signal-conditioning circuitry *in place* by applying a digital command. Most rudimentary sensors—particularly the commonly used electromechanical devices—cannot be adequately tested to ensure they are operating correctly. Even sophisticated sensors with accurate, continuous outputs can only be tested under controlled circumstances on precision vibration test-beds.

To self-test the ADXL50, a CMOS- or TTL-level digital stimulus is applied to the self-test input. This produces a voltage pulse which is injected into the feedback signal to the sensor. The resulting electrostatic force causes a deflection of the proof mass against the tethers as though it were responding to a negative full-scale acceleration. Though always available, self-testing would generally be programmed to occur each time at power-up.

AUTOMOTIVE APPLICATIONS

There are many on-board automotive systems that need a reliable, low cost way to measure acceleration. The most obvious and immediate application for the ADXL50 is in next-generation, single-point air-bag systems (see sidebar, "Air-bag Accelerometers"), where the ADXL50's output provides acceleration

information for the "is-a-crash-occurring?" decision to initiate the explosive charge to deploy the air bag.

Another automotive application of accelerometers related to safety is in automatic door-lock-release mechanisms. In the event of a collision that results in significant structural damage to the vehicle, passengers are often trapped in the vehicle, unable to be rescued, because the doors remain locked. Automatic door-lock release on impact could, in many instances, have prevented this; an accelerometer incorporated in the door lock would detect the rapid deceleration that occurs on impact, releasing the door locks.

Airbag systems and automatic door-lock release systems are forms of "passive safety" which make the consequences of collisions less dangerous. In addition, automobile companies are developing "active safety" systems which attempt to avoid collisions. Such systems include ABS (antilock brake system), ASR (acceleration slip regulation), and sophisticated new suspension systems that monitor and react to varying road conditions; in addition to increasing the level of safety, these also provide a more comfortable ride through improved vehicle control. *Active suspension systems* continuously monitor road conditions and vehicle dynamics and compensate through the use of power hydraulics and actuators in the suspension to restore the vehicle to a neutral orientation (or even a biased orientation, "leaning" into a corner for improved control). A simplified version is known as an *adaptive suspension system*, which responds to road conditions and vehicle dynamics by altering the response of the suspension components through changing such parameters as shock absorber or strut valving; the difference is that it does not employ restorative power devices. Both active and adaptive systems rely on measuring shock and vibration through monitoring wheel- and body motions—functions requiring the use of accelerometers.

An advanced form of vehicle control, derived from ABS/ASR systems, is based on monitoring *lateral acceleration*; when it is combined with longitudinal acceleration and vehicle velocity values, suspension settings may be altered side-to-side or front-to-back to make maximum use of the adhesion potential of the tires. Developments in this area include "yaw-rate" sensors, a special category of accelerometer which measures the rate of rotational velocity change. The resulting information may be used by the chassis control system to alter suspension settings as well as to more actively intervene in vehicle dynamics by selectively applying individual wheel braking (without driver input!). Selectively applying particular braking combinations applies yaw moments to counter undesired rotations of the vehicle. Various forms of such systems are already being used in racing applications such as "Indy" cars. As the cost of such systems is reduced, they will find use in vehicles for the general public.

The full-scale acceleration range of interest for suspension and "active-safety" applications is in the range of ± 2 g, for which Analog Devices is developing future versions of the ADXL50.

NON-AUTOMOTIVE APPLICATIONS

Acceleration is a fundamental physical quantity, manifested in many guises—gravity, vibration, and seismic activity are a few examples. Measuring acceleration continuously, accurately, and at low cost opens up numerous applications for the ADXL50 and future members of its family.

Manufacturers of portable computers continue to seek ways to make their products more rugged and reliable. The elements most prone to damage (and the catastrophic loss of stored information) are mass-storage devices, particularly hard-disc drives. The delicate mechanism that reads and writes information to the discs floats above them on a controlled flow of air; sudden movement can easily cause a problem, destroying data and drives alike. An accelerometer can detect the onset of potentially damaging shocks and institute "countermeasures" to prevent disc damage.

Many of us have had the disappointing experience of opening a large package to find the delicate contents damaged or destroyed due to mishandling. How did the damage occur, and who is to blame? If a package recorder—consisting of an accelerometer, a timer, and a data logger—were included with the consignment, these questions could be easily answered. Such recorders may soon be the norm for delicate, expensive items in transportation.

Military applications include smart detonation systems for missiles and bombs. Here an accelerometer forms part of the fuze system, detecting impact by the associated rapid deceleration. The continuously varying output of the ADXL50 would be quickly analyzed to establish the precise instant when the explosive charge should be detonated to produce maximum target damage.

The ADXL50 can also be used to monitor the health of machines. Rotating machines exhibit characteristic vibration signatures; as fatigue cracks or wear develop in portions of the machine, the signature changes. By continuously monitoring the machine's vibration, it is possible to be warned of imminent failure. Applications range from aircraft engines to heating, ventilation and air-conditioning (HVAC) systems.

FUTURE DEVELOPMENTS

The ADXL50 is Analog Devices' first micromachined acceleration sensor. It is the first of a family which will include a more sensitive device with a full-scale range of $\pm 2g$, a less-sensitive device for more-severe shock measurements, digital-output devices, and other formats. Also in development is a family of rate sensors. Future devices will also be available in a variety of packages.

Since the micromachined sensing element is so small, it is possible to incorporate several on a single chip, oriented to either the same or orthogonal axes. Thus monolithic dual-axis sensors can be constructed, allowing vector measurements of acceleration in the plane of the chip surface. Alternatively, two or more sensors can be aligned in the same plane, allowing for redundant sensing in fail-safe applications. In either instance, some sharing of the support circuitry (and perhaps even on-chip signal processing) will provide even greater economic value. Until multiple devices become available, the ADXL50's small size permits a high degree of compactness using separate devices.

The ADXL50 is available in a 10-pin T0-100 metal can with various grades, suitable for consumer, industrial, military, and automotive applications. DIP packaging is also in development. Pricing is \$38.50 in 100s, decreasing to <\$10 in large volumes.

The team that developed the ADXL50, headed by Dr. Richard Payne, includes Steve Sherman, Terry Core, Sarkis Ourfalian, Bob Tsang, Dave Quinn, Paul O'Brien, John Chang, Carl Roberts, Lew Long, and many others at ADI's manufacturing plant in Wilmington MA. □

AIR BAGS AND ACCELEROMETERS

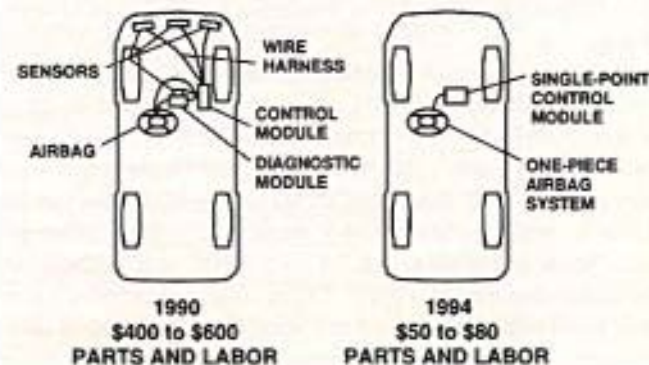
Automotive air bags have dramatically reduced fatalities and severe injuries of vehicle occupants involved in head-on collisions. As a result, many car makers have engaged to outfit all cars with them within the next 3 years; and legislation in the USA and elsewhere will mandate some form of passive restraint in all cars and trucks by 1995. This has resulted in a huge demand for a low-cost, highly reliable air-bag system.

Within an airbag system, the electronic control module makes the decision when to fire the airbag. Currently, most airbag systems in production use several electromechanical crash sensors, acting as on-off electrical switches, mounted at the front of the car. Their output is sent to the control module, which combines their outputs with that of an electromechanical "safing" sensor and decides whether to fire the airbag. The safing sensor is used to reduce the chances for a false deployment, which would be likely if only the output of the crash sensors were considered; the crash sensors have a fairly low trip point and can be fooled by potholes, etc. To trigger the airbag, at least one crash sensor and the safing sensor must close. These distributed systems are expensive to install, and reliability is compromised by the number of interconnections and the inability to self-test the sensors.

The new approach in airbags is to use a "single-point sensing system," where a single accelerometer (such as the ADXL50) is mounted in the passenger compartment, doing away with the crash sensors mounted at the front of the car and the associated wiring harnesses. Also, the output of the accelerometer is continuous, rather than on-off, with voltage proportional to the acceleration. This enables the system to use a more-sophisticated decision-making algorithm in its microcontroller to distinguish between a crash condition and other events—rather than relying on a majority vote of several switches. "Smart" algorithms use signal-processing approaches similar to those used in speech recognition and predictive methods to perform the decision.

An 8-mph (12.8 km/h) head-on crash into a solid wall should not deploy; a ≥ 12 -mph (19.2-km/h) crash should deploy. In some situations, the decision to fire the airbag has to occur in <15 ms from the start of the crash. The system's goal is to fire the airbag by the time the occupant has moved 5 in (0.13 m).

Single-point sensing provides significant cost reductions and increased system reliability through elimination of the many components and connections associated with multi-point systems. Furthermore, the continuous and linear output of the ADXL50 enables the use of more sophisticated deployment algorithms by the airbag system controller, resulting in a more accurate system with fewer unnecessary airbag deployments.



“Uncommon-Mode” High-Speed Video Feedback Amplifier with a Difference

AD830 has separate differential input and feedback circuits, combines wide bandwidth and high common-mode rejection

The AD830* is a wideband amplifier designed to reject high-frequency common-mode voltage and noise in differential line-receiver applications. It employs a powerful alternative topology, *active feedback*, with inherent advantages in handling differential signals and differing system grounds, level shifting, and low-distortion high-frequency amplification. With its ± 50 -mA minimum full-output-current drive capability, additional uses include buffering of ADCs and applications as a high-speed instrumentation amplifier and a high-speed level shifter.

As the simplified model of Figure 1 shows, an internal capacitor integrates the sum of the currents from a matched pair of differential-input transconductance (G_m) stages. In typical applications, the differential input signal is applied to one of the G_m stages, and negative feedback from the output to the other input closes the loop, which seeks to maintain the net current in the capacitor essentially at zero in the steady state. This current-balancing capability is akin to that of op amps, but since the currents are derived from differential voltages via the G_m stages, there is dynamic isolation between input and output circuits.

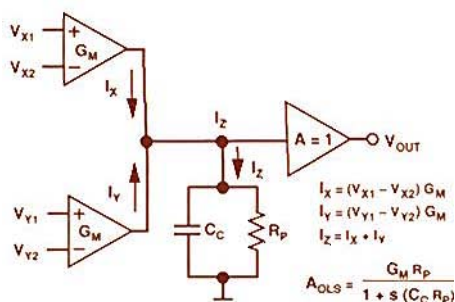


Figure 1. Open-loop amplifier topology.

Figure 2 shows the device's simple connection as a unity-gain difference amplifier/line receiver. The input is connected between X1 and X2 in either polarity, and the output is fed back to Y2. Y1 may be grounded directly—or connected to a source of offsetting voltage for level shifting. The circuit responds only to the differential input and feedback voltages, so it has excellent common-mode rejection, 100 dB, dc to 100 kHz, and 60 dB (55 min) at 4 MHz. Other characteristics include 50-MHz large-signal bandwidth (1 V rms); 100-MHz small-signal bandwidth (100-mV rms), with 0.1-dB flatness to 15 MHz; 530-V/ μ s slew rate and 35-ns settling time to 0.1% (4-V step); 0.05%/0.08° differential gain/phase errors (0 to +0.7 V, 4.5 MHz); and -72-dB total harmonic distortion at 4 MHz. DC performance includes ± 3 -mV max input offset voltage (± 5 -mV max, T_{MIN} to T_{MAX} , J and A versions); ± 13 - μ A max bias current and 1- μ A max offset current over temperature.

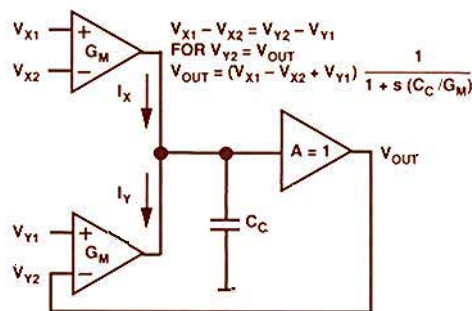


Figure 2. AD830 as a unity-gain difference amplifier (line receiver). For higher gains, attenuate the feedback. For level shifting, add an offsetting voltage at Y1.

The AD830's advantages over subtractor connections of op amps in differential applications include high common-mode rejection ratio, high-impedance inputs, symmetrical circuit behavior for gain of either +1 or -1, low sensitivity to the value of source resistance, equal impedances at the + and - inputs, inherently excellent high-frequency CMR, and freedom from having to use highly matched resistor sets.

For gains greater than unity, the feedback signal may be attenuated, in the same way that noninverting gain is achieved in operational amplifier circuits—but the differential signal input permits either polarity of gain. It is also worth noting that—unlike op amp circuits—performance of AD830 circuits is the same for positive and negative gains.

From the point of view of operational flexibility in systems, the availability of 2 pairs of signal terminals makes possible some analog signal-processing operations that would be cumbersome with operational amplifiers. For example, Figure 3 shows a circuit for summing two voltages at high impedance without using summing resistors.

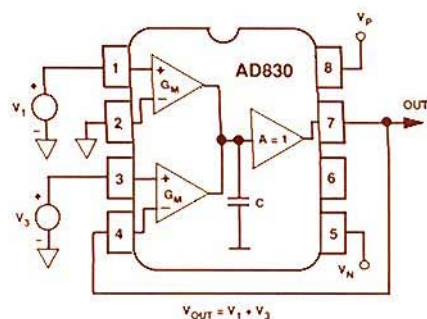



Figure 3. High-input-impedance summing amplifier without resistors.

The AD830 is characterized for performance with ± 15 -volt and ± 5 -volt supplies, but its offsetting capability means that it can also perform well with single supplies from +10 to +30 V. Performance/temperature grades include J and A for commercial and industrial temperature ranges, and S for -55 to +125°C. Packages include 8-pin plastic mini-DIP, Cerdip, and SOIC. A 16-page data sheet includes a variety of application suggestions and 28 families of performance curves. Prices start at \$2.42 (1000s).

The AD830 was designed by Analog Devices Fellow Barrie Gilbert at ADI's Northwest Labs, Beaverton, OR. 

*Use the reply card for technical data. Circle 2

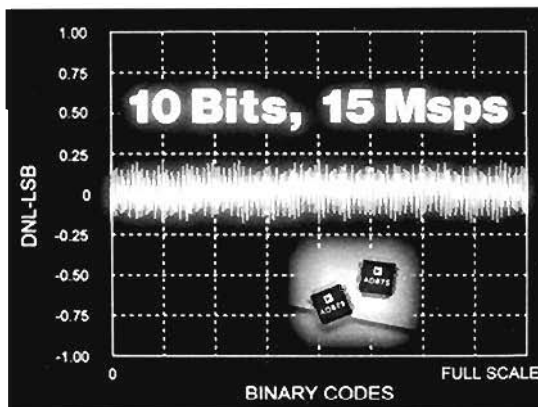
CMOS 10-Bit, 15-MHz A/D Converter for Imaging Applications

AD875 uses a single +5-volt supply and dissipates only 185 mW (<50 mW in standby)

The AD875* is a 10-bit, 15-MHz A/D converter designed to digitize high-speed stepped signals, such as the outputs of charge-coupled devices, infrared imagers, and multichannel data-acquisition systems. Implemented in CMOS, it has low power requirements—185 mW typical, 235 mW max, and even less (<50 mW) in the power-down standby mode—an important feature in portable battery-operated systems, such as camcorders and electronic still cameras.

The converter guarantees no missing codes over the full temperature range (0 to +70°C), is packaged in a tiny 48-pin flatpack, and can operate from a single +5-volt supply. Its digital I/O can interface with either +5-V or +3.3-V logic. The speed and precision of the AD875 are ideally suited for digitizing sampled video signals directly from charge-coupled devices (CCDs) in color scanners, digital copiers, and electronic still cameras.

Using a multi-stage pipelined architecture (Figure 1) with output error correction, the AD875 achieves differential nonlinearity of ± 0.4 -LSB (1.0 max) over the entire range of input and temperature, and small-signal differential nonlinearity (DNL) of 0.8 LSB max—an important advantage in imaging systems.



series resistance, Force and Sense terminals are provided at the ends of the reference ladder so that it can be driven using Kelvin connections. The power-supply connections, with their associated grounds, are separated into three components—analogue, digital, and digital I/O buffers, to permit a flexible choice of logic voltage and to optimize the AD875's performance.

IMAGING SYSTEMS

While the specifics of a particular system may vary, most imaging-system architectures will employ some or all of the building blocks shown in Figure 2. The image sensor, often a charge-coupled device (CCD), transforms light intensity to a sampled electrical output. The resulting stream of pixel values is conditioned by a clamp/sample-and-hold circuit, sometimes referred to as a *correlated double sampler* (CDS). A gain block sets signal levels to normalize the signal range to the A/D converter's optimum full-scale input range. DC restoration is used to remove any errors in the signal's dc level due to ac coupling and dc drift. Since the input to the converter is a rapidly stepped dc voltage, a sample/hold is unnecessary (except for the internal SHAs used as part of the multistage pipelined conversion process). After conversion to digital, the signal is subjected to digital processing that depends on the application.

Depending on resolution and bandwidth requirements, color information may already exist in the sensor signal (camcorders), the RGB signals may be separately acquired and multiplexed ahead of the converter for color scanners, or three independent channels may be converted in parallel for high-resolution color video.

The AD875 is specified for the 0 to +70° commercial temperature range and is housed in a space-saving 48-pin thin quad flatpack (TQFP). An evaluation board is available. Price of the AD875 in 1000s is \$21.50.

The AD875 was designed by a team led by Mark Martin and Chris Mangelsdorf at ADI's Wilmington facility.

*Use the reply card for technical data. Circle 3

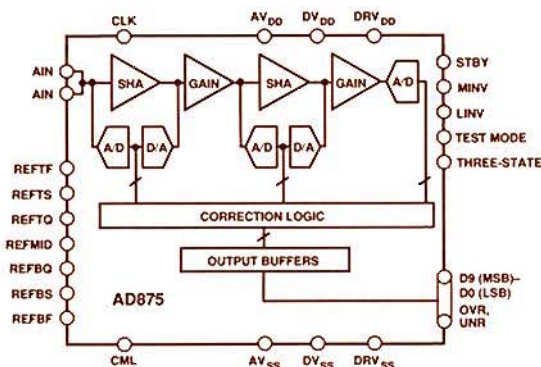


Figure 1. AD875 block diagram.

Besides power-down, additional functions to reduce system cost include 3-state outputs, underrange and overrange flags, and a flexible choice of output formats, including positive- and negative-true binary and twos complement. To minimize errors due to

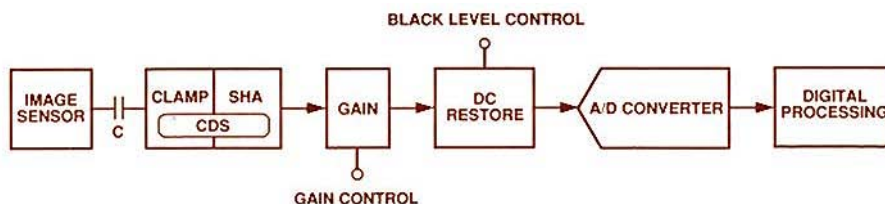


Figure 2. Typical imaging system.

Increase Laser Printer Resolution with Win-Win Chip—No Tradeoff Worries

Pulse-width modulator is superior to super-pixel technique for gray-scale—and doesn't need a higher-resolution engine

by Bill Schweber

The AD9560* pulse-width modulator (Figure 1), is a monolithic IC designed specifically to enable laser-printers to provide increased resolution and more realistic "gray-scale" images, even with a standard 300-dot-per-inch (dpi) "engine". It does this by setting the laser-diode's excitation pulse width and position, for each pixel, in proportion to a control word supplied by the printer controller. This permits control of both area and placement of toner for each final printed dot. The AD9560 can also be applied in color printers; in fact, it has already been designed into several prototype monochrome and color printer systems.

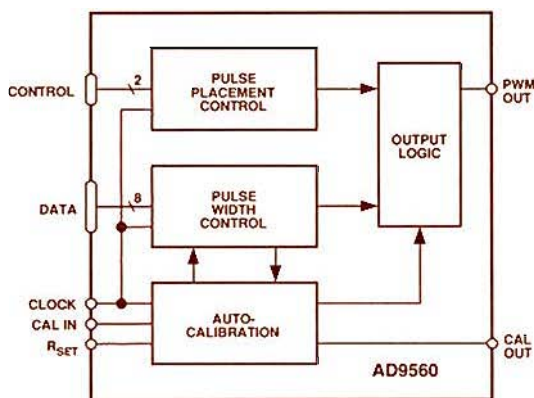


Figure 1. Block diagram of the AD9560.

The AD9560 uses a similar architecture to members of the AD9500 digitally programmable time-delay generator family (*Analog Dialogue*, Vol. 22-1). Like the AD9505, it is designed for pulse reprogramming on each cycle. Complete and self-contained, the AD9560 connects to the laser-diode driver circuitry in the printer, which would require a profusion of discrete circuitry—and at less power and expense for the same functionality. It



requires only a single external resistor to match its nominal full-scale range to that of the dot clock. An on-chip autocalibration circuit fine-tunes the range and compensates for lot-to-lot variations of the on-chip timing circuits.

With the AD9560, pulse width and pulse placement can be changed on every clock cycle at clock rates up to 50 MHz. Output pulsewidth is proportional to the value of a parallel 8-bit data input, while pulse placement (beginning, middle, or end of the clock period) is set by two control lines.

For mixed-mode printed images, which combine the variable tones of graphics with the black-or-white pixels of solid text, it is useful to disable the modulation and force full on/off operation during the text portions. This is easily achieved by entering a 00 or FF (hex) code, which sets the IC output to logic zero or logic one for the entire clock cycle.

The relationship between the system dot clock, data, position control codes, and resulting output to the laser-diode driver is shown in Figure 2 for some data and control combinations. The figure is idealized in that it does not show internal propagation or buffer delays, which must of course be accommodated in the system design.

EVALUATION BOARD

A complete and compact evaluation board (3.8 × 3.2 inches, 97 × 84 mm) is available to examine the performance of the AD9560 (Figure 3). This board requires a +5-V supply, a pulse generator for the dot clock, and an oscilloscope for viewing the

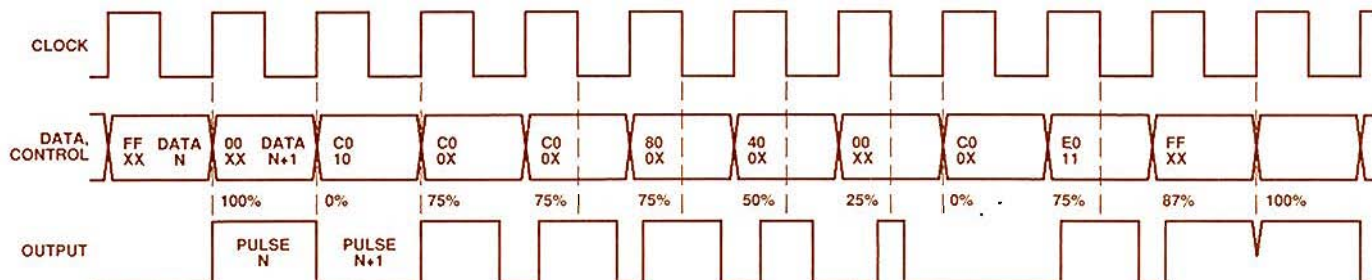


Figure 2. Example of timing diagram.

output pulse. Output duty cycle and pulse position are user-settable manually via DIP switches on the evaluation board and dynamically via a 25-pin connector.

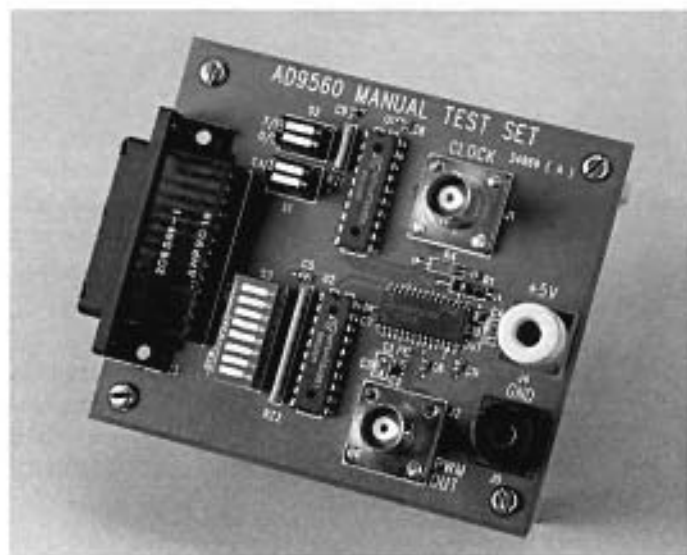


Figure 3. AD9560 evaluation board.

The AD9560 is available in 28-pin DIP and SOIC packages, for the 0° to +70°C temperature range. Price is \$15.30 (1000s) for the SOIC package.

The AD9560 was designed by Edward Jordan at Analog Devices' Greensboro, NC facility.

GRAY-SCALE TECHNIQUES

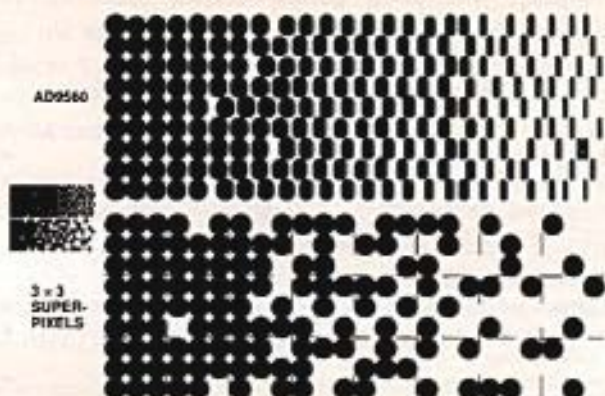
For video displays (CRTs), achieving gray scale images is relatively straightforward: just control the intensity of each displayed pixel. This is done by modulating the CRT electron beam intensity, through an all-analog circuit in conventional TV, or a DAC in a PC system. The brightness of the pixel is closely proportional to the intensity of the electron beam. This is equally true for monochrome and the red-green-blue beams of color displays.

For printed images, the situation is very different. Monochrome printing is done with inks—or toner, in the case of the laser printer—having a chosen intensity and hue, and there is no convenient way for the intensity signal to directly modulate the intensity of the medium itself. But the inherent averaging ability of the eye and brain for small parts within a larger whole offer a solution: vary the portion of the pixel area to which the medium is applied; the eye responds to the reduced proportion of black (or other single-color) area as though it were solidly printed with reduced intensity. [For a familiar example of this, look at the various shadings of a newspaper photo through a magnifying glass.]

The "sub-pixel" approach uses numerous small pixels to represent each data point and adjust the local number of black (on) dots relative to the unprinted white (off) area to provide the required intensity. The eye then integrates these into an

equivalent gray-scale value. But this technique has a downside. The larger number of smaller dots required to give adequate gray-scale resolution without losing spatial resolution requires a faster clock for the pixel control circuitry to fit the increased number of dots into the time for one standard dot. It is somewhat costly because it requires, along with higher-speed digital components and special high-speed layout considerations, a high-quality printing process to achieve the spatial resolution.

Gray-scale is often approximated on the present generation of printers, using full-size on-off pixels, with a "super-pixel" technique: as shown below, it computes the average intensity over a group of individual pixels (between 8 and 16) and then varies the number of "on" pixels to produce that intensity, averaged over the group. It is essentially similar to the approach described above, but with greatly reduced spatial resolution and provides only low gray-scale resolution (8 to 16 levels), equivalent to a newspaper photo.



In contrast, the pulse width and -position modulation of the AD9560 directly controls intensity by varying the size and incremental position of the ink deposited in each pixel in analog fashion without involving digital tricks, such as adding pixels or involving computations with adjacent pixels. Instead, it allows the duty cycle for each pixel to be varied between 0 and 100%, thus varying the energy absorbed by the photoconductive drum of the laser printer. In turn, more or less toner is attracted to each dot according to its energy level, and gray scale toning is achieved on a dot-by-dot basis. The resulting image quality is comparable to a "slick" magazine image.

In addition to pulsedwidth, the AD9560 allows the pulse position within the clock period to be set to the leading edge, center, or trailing edge of the clock, an additional degree of freedom that can be used by the printer software to enhance the perceived appearance of the resulting image, as the above idealized example demonstrates, for a gradation from 100% down to 20% gray scale. Thus, with 8-bit control of the dot area (254 levels between all-on and all-off) and 3 position-alternatives, a pixel may be printed in any of 764 different ways, as determined by the processing of the digital image-intensity signal and the resulting 10-bit intensity-control word.

*Use the reply card for technical data. Circle 4

Video RAM-DACs Offer Unprecedented Resolution, True-Color Screen Images

ADV715x Series features triple 10-bit resolution, with speeds up to 220 MHz

by Bill Slattery

Combining three 10-bit video digital-to-analog converters and the associated color-palette RAM in a single package, the ADV7150 series* of RAM-DACs is industry's first monolithic solution that provides true color and gamma correction. These software-compatible ICs—capable of displaying 16.8 million colors at one time, from a palette of over 1 billion colors, offer 24-bit true-color performance with 30-bit gamma-corrected operation. Three devices provide a choice of specialized features (Table 1).

Table 1. Features of the AD715x family

Feature	ADV7150	ADV7151	ADV7152
24-bit "gamma" true color	•		•
24-bit "standard" true color	•		•
8-bit "gamma" pseudo color	•	•	•
24-bit "standard" pseudo color	•	•	•
15-bit true color	•		•
220 MHz—true color	•		•
220 MHz—pseudo color	•	•	•
Triple 10-bit DACs	•	•	•
4:1 multiplexing	•	•	•
2:1 multiplexing	•	•	•
1:1 multiplexing	•	•	•
160-lead QFP package	•		
100-lead QFP package		•	•

The ADV7150/ADV7152 are the industry's first monolithic RAM-DACs capable of delivering 24-bit True-Color performance at rates up to and including 220 MHz. The AD715x series holds another industry first with its triple 10-bit RAMs and triple 10-bit DACs [For additional discussion of video DACs and color images, see *Analog Dialogue*, Vol. 24-3, pp. 3-6 and p. 7.]

Such high-resolution displays are used to show both fine detail (icons, menus, images) and subtle color shading, to capture the true image accurately. Generally, the standard triple 8-bit video display is not sufficient for applications such as full color pre-press (preparation for color printing). Although the average user will not be aware of differences between 8-bit and 10-bit color, the professional artist or color printer will appreciate the benefits.

Speed and Resolution: Increased screen resolution is the prime factor driving the increasing speed requirements of video RAM-DACs, since a high update rate is needed to avoid flicker (the *de facto* standard is 60 Hz, but this figure is destined to increase to between 70- and 80 Hz to minimize eyestrain caused by "peripheral flicker"). Table 2 shows the resolution values required for different graphics systems and the pixel clock rates needed to achieve them.

But the speed of the RAM-DAC determines only the X-Y (spatial) resolution of the graphics system, i.e., the number of pixels/frame



and frames per second. The DAC resolution, in bits, adds color depth to the displayed image. More DAC bits allow the system to provide more shades of each primary color, resulting in many more combined shades of color and much truer color definition.

The ADV7150 and ADV7152 are 24-bit true-color devices, with three 8-bit control inputs, one for each of the red, green, and blue channels. This provides 256^3 (nearly 17 million) addressable colors. The pseudo-color ADV7151 can display an image with the same number of pixels (resolution) but with a choice of only 256 colors per frame.

Applications requiring the same pixel resolution may have differing color-resolution needs. For example, the needs of engineering wire-frame modeling, IC circuit design, and black-and-white desktop publishing can be satisfied with 256 colors. However, volume visualization, 3-D solids modelling, and full color pre-press must have available the more than 16 million colors that the ADV7150 and ADV7152 offer. For example true display of the various shades of green and red give an apple's image depth and realistic image quality.

These workstation RAM-DACs differ in their architecture from industry-standard devices for PCs (the ADV47x series) by their on-board multiplexers (Figure 1). Internal multiplexers eliminate the need for multiplexing at the system level. Since the display needs a video rate of, for example, 160 MHz, but today's fastest video RAMs operate at speeds of up to 40 to 50 MHz, the graphics circuitry must include multiplexing to accommodate the difference between what a single video RAM can provide and the actual RAM-DAC (and screen) requirements.

Four 40-MHz video RAMs can be directly connected to the input of an ADV7150 or ADV7151 and multiplexed at 160 MHz to yield the required video bandwidth. The on-chip multiplexer does have a downside, the high pin count for these devices—since 24-bit true color requires 24 input pins. Thus, four multiplexed inputs require 96 pins, in addition to connections for control, power, and other functions. The ADV7150's pixel input ports can also be multiplexed at rates of 2:1, and 1:1.

The ADV715x series is also unique in that it has on-board clock control circuitry and does not require additional (and expensive) control ICs. The need for a separate pixel/load clock synchronizer

Table 2. RAM-DAC resolution, clock speed, and applications.

Screen Resolution (pixels)	Pixel Clock Rate	Application
1024 × 768 (76 Hz update)	80 MHz	Super VGA
1152 × 870 (76 Hz update)	100 MHz	Macintosh 21" screen
1152 × 900 (76 Hz update)	106 MHz	Sun SPARCStation
1280 × 1024 (76 Hz update)	135 MHz	DEC, HP, IBM workstation
1600 × 1280 (60 Hz update)	170 MHz	High-end workstation
1600 × 1280 (76 Hz update)	220 MHz	Imaging workstation

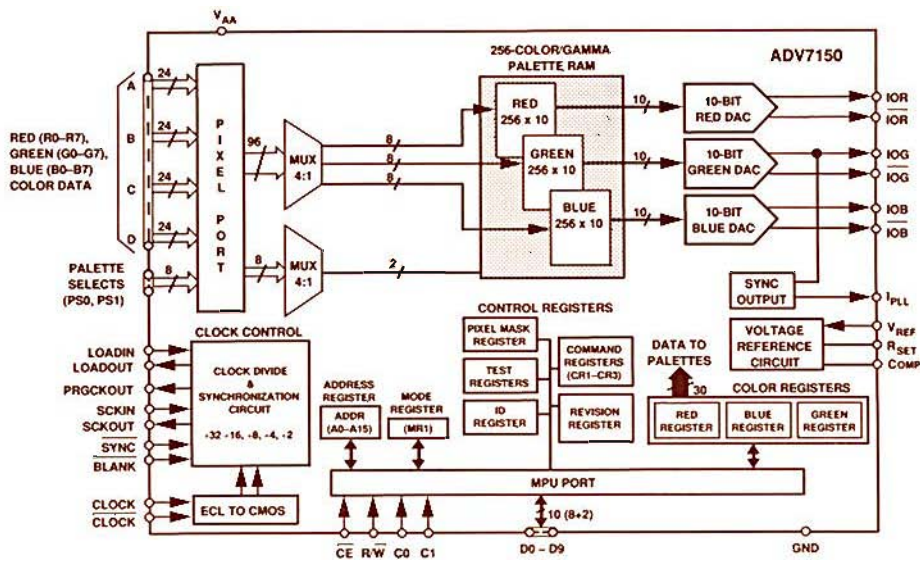


Figure 1. Block Diagram of the ADV7150.

is eliminated by a divided-down, synchronized "loadout" clock. All necessary signals, including data-transfer signals, such as LOADOUT, PRGCKOUT, & SCKOUT are available (Figure 2).

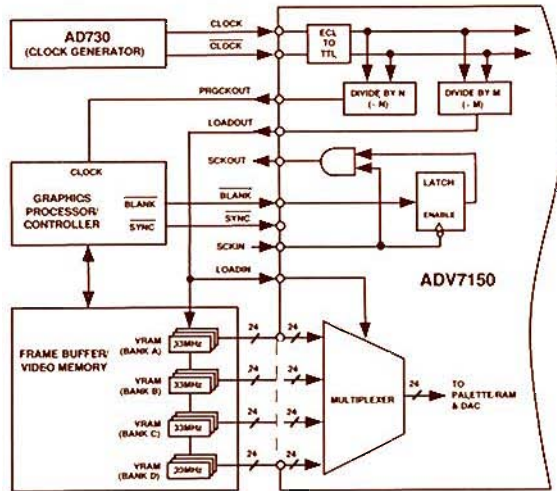


Figure 2. Frame-buffer interface.

GAMMA CORRECTION

While an increased number of DAC bits is important to more closely approximate the eye's ability to resolve differences in the displayed image, it is not a complete solution. Unfortunately, the response of the CRT's color phosphors to the electron beam that impacts them is not linear. This non-linear response, which is seen by the eye as deviation from the intended color value, is called the gamma function, where γ is an exponent in the approximate relationship between the electrical intensity input and intensity of the light produced by the phosphor:

$$I_{CRT} = (I_{IN})^\gamma \quad 2.0 < \gamma < 2.8$$


If the value of γ is known for each primary color (red, green, blue) the gamma error can be compensated for by using a $1/\gamma$ factor to correct I_{IN} . [Note that conventional television has analog gamma correction circuit built into the camera to correct for this problem.

Also, it's worth noting that in TV the intensity modulation is produced by an analog signal with the "infinite" resolution of continuous response, rather than with a digital input and a DAC that responds with "bits of resolution"!]

In digital systems with limited resolution, there is a conflict between the linear relationship of binary values and the requirements for more bits to implement gamma correction accurately at low values of intensity. The ADV715x series is inherently more suitable with its 10-bit instead of 8-bit resolution. The ADV715x chips contain lookup tables for γ correction.

An interesting and prominent application of this 10-bit DAC technology is in systems for initial and periodic correction and calibration of CRT color monitors using feedback techniques. With a measuring device placed on the monitor screen, the system inputs known "signals" to the display under test, measures the resulting color image, and sends this information back to the system. A color matching calibration algorithm (gamma correction) then calculates correction factors, and the contents of the color palette in the system's RAM-DAC are modified accordingly. This approach benefits by the use of 10-bit display DACs because the measuring system should have higher resolution than that being measured.

The ADV715x series of RAM-DACs are fabricated in CMOS and require a single +5-V supply. Current consumption is <350 mA for the fastest ADV7150 (and less for slower grades). For all three devices, analog video outputs are RS-343A and RS-170 compatible. The ADV7150 is packaged in a 160-lead plastic quad flatpack (PQFP); the ADV7151 and ADV7152 are in 100-lead PQFPs. The ADV7150/51/52 are available in 85, 110, 135, 170 and 220-MHz speed grades. They range in price (1000 pieces) from \$71/\$51/\$69 for the 85-MHz grades to \$167/\$121/\$163 for the fastest (220-MHz) grades.

The ADV715X series was designed by a team led by Tim Cummins at Analog Devices' Limerick, Ireland facility. 

*For technical data on these parts, use the reply card. Circle 5

Fast, Accurate, Monolithic Sampling A/D Converter

10-Bit, 40-MSPS AD9040A has 54-dB SNR at 10 MHz. Evaluation board permits quick performance testing

The AD9040A* is a complete monolithic 10-bit sampling A/D converter with on-chip track-and-hold, voltage reference, and timing circuitry. Designed for low cost, high-performance, and relatively low-power dissipation (940 mW typical, 1.1 W max), it requires only an encode signal to achieve sampling rates as high as 40 MSPS. When sampling a 10.3-MHz analog input at 40 MSPS, its signal-to-noise ratio (including distortion) is typically 55 dB (8.8 ENOB), 51 minimum.

Typical applications include beamforming in ultrasound medical imaging (requiring low power, wide dynamic range, and low cost), professional video image processing (e.g., special effects and tape recorders), digital communications (wireless LANs and cellular base stations require wide dynamic range and bandwidth to pick out small signals of interest in the presence of potentially large interfering signals), digital oscilloscopes, and advanced television (MUSE) decoders.

The AD9040A employs a two-step subranging architecture with digital error correction (Figure 1). The analog input is applied to a high-input-impedance track-and-hold, which holds the analog value when an Encode strobe is applied. The 2.5-volt precision on-chip bandgap reference can be used to avoid external references, allowing denser packing of ADCs for multichannel applications. The device requires power of +5 V at 89 mA (105 mA max over temperature) and -5 V at 87 mA (100 mA max).

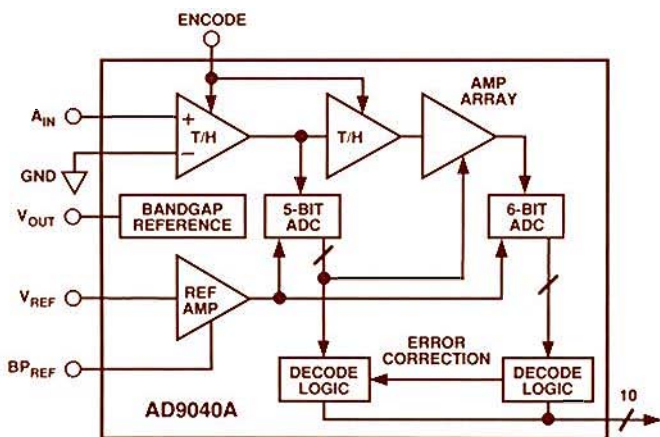
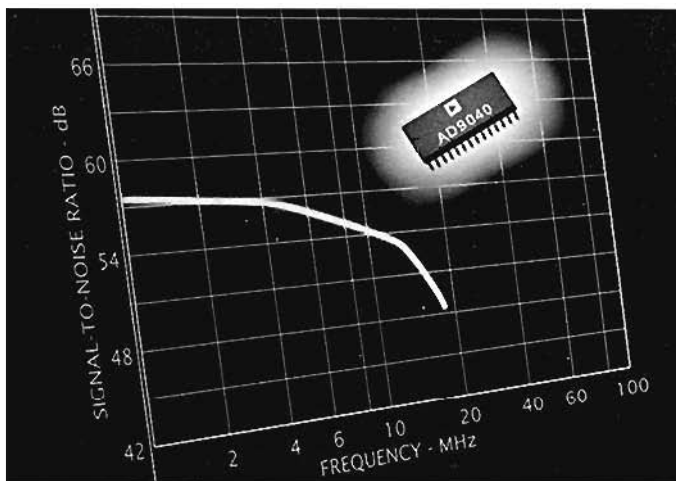


Figure 1. Block diagram of the AD9040A.

The high input impedance and full-scale input range of 2 V p-p eliminate the need for external buffers in many applications. The digital inputs and outputs are CMOS compatible, allowing direct interfacing with ASICs. An out-of-range output goes high when the analog input goes 1 LSB beyond the maximum or minimum end of the ADC's input range.



The AD9040A is designed to be sampled at rates from 2 to 40 MSPS, with a minimum specified range of 10 to 40 at 25°C. Typical sampling aperture delay is 1.9 ns, with jitter of 7 ps, rms. The output propagation delay is 14 ns max over temperature.

Dynamic specifications include maximum second- and third-harmonic distortion (Figure 2) of -56 and -58 dBc respectively, at 10.3 MHz, and typical two-tone (2.3 and 2.4 MHz) intermodulation distortion rejection of 62 dBc. In video applications, its maximum differential gain and phase errors are 1.0% and 0.5°.

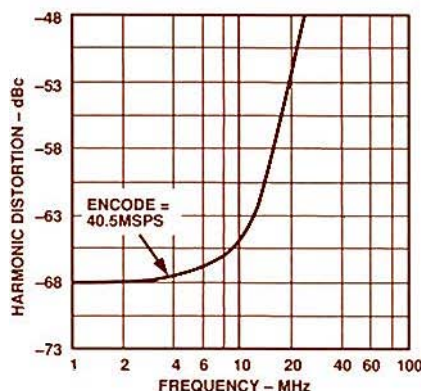


Figure 2. Harmonic distortion as a function of frequency at 40.5 MSPS sampling rate

The analog input, with 5 pF input capacitance and 200-kΩ minimum resistance, accepts signals with bandwidth up to 48 MHz. Maximum offset voltage over temperature is ±30 mV, and maximum bias current is 25 μA.

Accuracy specs include no-missing-codes guaranteed over temperature, maximum differential and integral nonlinearity of 2.5 LSB over temperature, and maximum gain error of 2% of full scale over temperature.

An evaluation board is available—including a reconstruction DAC and latches. The AD9040A is available in 0 to +70°C (28-pin plastic-DIP and SOIC) and -25 to +85°C (ceramic-DIP and gull-wing surface-mount) versions. Prices start at \$50 in 100s; the evaluation board is priced at \$250.

The AD9040A was designed by a team led by Frank Murden and Carl Moreland, of our Greensboro NC facility.

*For technical data, use the reply card. Circle 6

High-Performance ICs in Single-Supply Analog Circuits—Design Issues and Application Examples

by Walt Jung and James Wong

As system designers increasingly use single-supply power for both analog and digital circuits, they face challenges if they must obtain the kind of performance they are used to at higher voltages—and increased challenges if they seek to better it. This article examines some typical precision analog functions with op amps and other devices, using chips and application techniques designed to produce maximum benefit on single low-voltage (3-5-volt) supplies at low power. We first consider device limitations, then discuss examples of application circuits.

DESIGN ISSUES

Selecting Amplifiers

The choice of amplifier (or other analog chip) is a critical step toward a successful single-supply design. A source of helpful information, Table 1 lists typical specs of currently available Analog Devices op amps suitable for use on single supplies ≥ 3 V, in order of increasing power consumption per channel. Although most of these devices work over much wider voltage ranges, as well as on dual supplies, our emphasis is on their low-voltage single-supply behavior. Characteristics listed include single-supply voltage range and input- and output (grounded-load) common-mode ranges, for supply voltages ≤ 5 V. As the table indicates, many of the amplifiers are available as singles, duals, and even quads; and most come in both DIP and SOIC packages. Also listed are (5-V) quiescent currents per amplifier channel, output drive current, and basic dc & ac specifications. The following detailed discussions will provide further insight into specific amplifier design features.

Reduced Signal Range

Most op amps in use today are designed for traditional ± 15 -V supplies, which allows ample input common-mode (CM) voltage range, as well as a wide output range—typically ± 10 V for both. Because power conservation is a major reason for using them, single-supply systems often have closely restricted supply voltage, for example, +12 V down to +5 V, as low as +3 V, and even in some cases +1.5 V. At these low voltages most standard dual-supply op amps cease to function at all, while some may still operate with degraded specifications. Until recently, low-voltage amplifier choices have been limited.

General purpose 741s & 1558s, and most FET-input amplifiers operate on supplies as low as ± 5 V (10 V total). Precision amplifier families such as OP-07 or OP-27 types don't work below ± 5 V. Types from some selected families may be used over regions of this voltage spectrum; for example the AD705 & OP-97 families are useful down to ± 2.25 V (4.5 V), and the AD817 wideband op amp is spec'd for +5-V use. But in general, only amplifiers that are specifically designed for single-supply use will function without major limits in CM range and output swing below +10 V. Examples are the LM324/LM358 families as general-purpose modest-performance single-supply types, and the devices of Table 1 for precision uses.

Watch Out for Input/Output Swing Limitations

Amplifiers designed for ± 15 -V operation typically need 2 to 5 V of headroom at input and output, with respect to both supply rails. Even more-flexible dual-supply designs, such as the AD705 & OP-97 families, approach only to within 1 V.

In low-voltage (3- to 5-V) single-supply applications, such headroom requirements become critical limitations to linear operation over even modest signal swings. For this reason, single-supply amplifier input stages are designed to remain fully linear, even when the input CM voltage is at the negative rail, or 0 V. Differential input-stage architectures allowing this involve PNP bipolars, CMOS (or PMOS) inputs, and N-channel JFET inputs. The various devices result in differing input bias currents, noise voltages/currents, and offset voltages/drifts. All the devices listed in Table 1 can operate with $V_{IN} = 0$ V; at the upper end of the CM range, some devices can go to within 1 V of the rail, while others may need 1.5 V.

Table 1. Op-Amp Chips Compatible with 3- and 5-Volt Single-Supply Systems

Device/s	Amplifier ⁽¹⁾ Channels	Supply ⁽²⁾ Range (V)	V_{IN} Range 0 to (V)	V_{OUT} Range (V) to (V)	Bandwidth (kHz)	Stew Rate (V/ms)	Quiescent ⁽³⁾ Current (μ A)	I_{OUT} Range (mA)	Offset Voltage (μ V)	Bias Current (nA)
OP-90/290/490	1/2/4	1.6-36	$+V_S - 1$	0.6, 4.0 ⁽⁶⁾	25	10	20	± 5	125	4
OP-22	1	3.0-30	$+V_S - 1.5$	0.7, 4.1 ⁽⁶⁾	200 @ 10 μ A ⁽⁴⁾	80 @ 10 μ A ⁽⁴⁾	10-100 ⁽⁴⁾	$\pm .02$ to ± 20 ⁽⁴⁾	400	3 ⁽⁴⁾
OP-20/220/420	1/2/4	5.0-30	$+V_S - 1.5$	0.7, 4.1 ⁽⁶⁾	100	50	45	± 0.4	300	16
OP-32 ⁽⁵⁾	1	3.0-30	$+V_S - 1.5$	0.7, 4.1 ⁽⁶⁾	1000 @ 100 μ A ⁽⁴⁾	300 @ 100 μ A ⁽⁴⁾	15-450 ⁽⁴⁾	$\pm .02$ to ± 20 ⁽⁴⁾	400	4.5 ⁽⁴⁾
OP-295/495	2/4	3.0-36	$+V_S - 1$	0, $+V_S$	75	30	150	± 3.5	300	8
OP-80	1	5.0-16	$+V_S - 1.5$	0, 3.7	300	400	325	+40, -20	400	0.0006
AD820/822	1/2	3.0-36	$+V_S - 1$	0, $+V_S$	1900	3000	700	± 15	300	0.002
OP-292/492	2/4	5.0-36	$+V_S - 1$	0, $+V_S - 1.5$	4000	300	1000	± 8	500	350
OP-183/283	1/2	3.0-30	$+V_S - 1.1$	0, $+V_S - 1.1$	5000	10000	1200	± 20	300	400
OP-113/213/413	1/2/4	4.0-36	$+V_S - 1$	0, $+V_S - 1$	3500	1000	1400	± 30	100	500
SSM-2135	2	4.0-36	$+V_S - 1$	0, $+V_S - 1$	3500	1000	1400	± 30	200	300

NOTES

¹Number of amplifiers on chip: 1—single amplifier, 2—dual, 4—quad.

²Total supply voltage span, single or dual.

³Per amplifier, using +5-volt supply.

⁴Varies with I_{SET} .

⁵ $A_{v(mia)} = 10$.

⁶ V_{OUT} range can be extended to include 0 volts, using pulldown resistor.

With the exception of parts specified with output swing of 0-to- $+V_s$ (or "rail-to-rail"), most op amps swing to within only 1-to-2 V of the positive rail. So, on supplies of 5 V or less, output swing is greatly reduced in relation to the supply. Even if the input noise floor were to remain constant (which it seldom does), signal-to-noise (SNR) and dynamic range suffer. The sidebar, "Single-Supply Amplifier Output Stages," covers some key factors in single-supply output stage design, and helps differentiate the devices of Table 1 architecturally.

Quiescent Current Drain

Aside from basic cost factors, another fundamental reason for single-supply designs is to conserve power, since they are quite often used in battery-operated equipment. So not only are they designed to perform at very low voltage, but they must also have low quiescent current per channel (I_Q). Unfortunately, low-current designs require basic tradeoffs; in general, sacrifices involve bandwidth, slew rate, and input noise voltage.

Standby current drain (no signal) per amplifier can often be used to qualify a device for critical system power conditions. In the absence of a standard industry definition, we call devices with I_Q of ≤ 1 mA/channel low power, and those with I_Q of ≤ 100 μ A/channel micropower. Many of the devices shown in Table 1 meet one or more of these criteria.

Noise Tradeoffs

Bandwidth versus noise is a highly likely tradeoff, as demonstrated by the following examples: the OP-295/OP-495 has input voltage noise of 51 nV/ $\sqrt{\text{Hz}}$ at 150 μ A/channel, the AD820/AD822 has 12.5 nV/ $\sqrt{\text{Hz}}$ at 700 μ A/channel, and the OP-113/213/413 family has noise of 4.7 nV/ $\sqrt{\text{Hz}}$ at 1.45 mA/channel. Lower noise can be attained at the price of increased current.

Reduced Bandwidth

In a low-power design environment, engineers are forced to face not just generally slower speed in the op amps, but also higher circuit impedances, which themselves can set bandwidth restrictions.

Again, tradeoffs exist. For example the bipolar-input OP-295 has an attractively low current drain of 150 μ A/channel, but the bandwidth is 75 kHz with SR of 0.03 V/ μ s. Where more speed is needed, a FET-input AD820 could be considered, with a 1.9-MHz bandwidth and 3-V/ μ s SR, at the cost of increased current, 700 μ A/channel. Both of these dual devices have rail-to-rail output stages. The OP-183/283 achieve 5 MHz and 10 V/ μ s, but with current of 1.2 mA/channel.

"Where Is Ground?"

This issue can become quite important in single-supply op amp ac-coupled circuits, since a circuit designer can arbitrarily choose any value for this "false" or pseudo-ground return level. The best choice depends on the application, but a flexible choice of amplifier circuits—and devices that can be used in them, helps make signal referencing easier, particularly in cases where substantial dynamic (i.e., ac) current is present.

Possible choices here range from a simple ac-bypassed resistive divider to fully buffered op amp follower stages that provide the lowest wideband dynamic impedance. A well bypassed noise-free divider is suitable for high-impedance loads, where the dynamic current is low. When dynamic currents are higher, the divider can be buffered with a follower-connected op amp.

AMPLIFIER OUTPUT STAGES

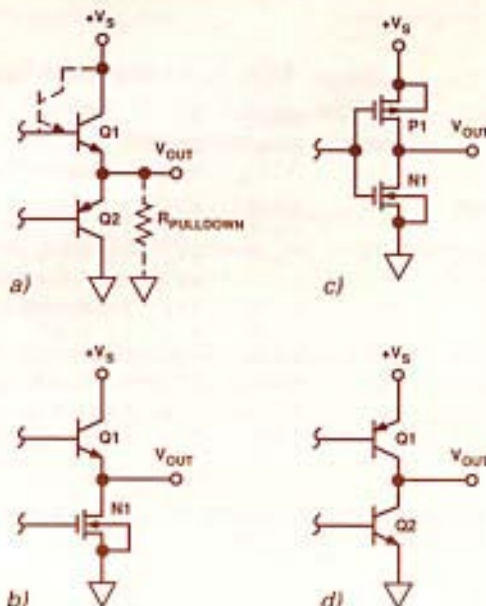
While output swing can be very important in single-supply applications, not all single-supply amplifier outputs are designed to swing all the way to the negative rail (ground). Some may swing to within a diode drop (≈ 0.6 V), others to within a few tens of mV. Only a few swing to within 1 mV of the negative rail—and a precious few swing nearly to both supply rails.

To understand which device types work best in applications for which output swing is critical, a designer needs to know about the design of the output stage. These vary widely in detail, so knowledge of their architecture can be critical to an informed selection. The figure illustrates a sampling of some output-stage topologies used in ADI single-supply amplifiers.

The complementary emitter-follower stage of (a), employing bipolar transistors (an NPN transistor for Q1 and a PNP for Q2), can swing to within a diode drop of each rail, at best. It cannot pull right to ground without outside help, such as by adding R_{PULLDOWN} , as noted within Table 1 (Note 6). This optional external resistor (which can also include the op-amp's gain-set resistors) bypasses the lower PNP, with its saturation limitation. This technique allows output linearity to ground only when sourcing current; and it can also raise overall dissipation, which may be excessive for sustained high-level outputs. Amplifiers with this type of output have their uses, but should be carefully applied to minimize tradeoffs in single-supply applications. This stage is used in the OP-90/290/490 families, among others.

The output stage of (b) uses a bipolar emitter follower and NMOS common-source. Though inherently asymmetric in terms of voltage swing, it uses the NMOS pulldown to achieve very low saturation voltage to ground. However, saturation voltage to the positive rail is ≥ 1 V. This stage is used in the OP-113/213/413 families, as well as in the AMP-04 single-supply instrumentation amplifier.

The CMOS stage of (c) is fully complementary and offers a resistive connection to the supply rails for both high and low output, viz., a swing of 0 to $+V_s$, or "rail to rail." With appropriate low- R_{ON} devices for P1/N1, the saturation drop to



either rail can be ≤ 1 mV at low currents. Because this stage is inherently Class AB, the amplifier design must carefully control the static currents in P1-N1 to maintain low quiescent current. For output currents of a few milliamperes, this type of output stage is effective and quite versatile due to its wide swing. This stage is used in the OP-295/495 families and others.

The complementary-bipolar common-emitter stage of (d) is another rail-rail output stage. Saturation drops range from a few millivolts to a couple of hundred mV, over current ranges of up to about 20 mA. Like the CMOS rail-to-rail output stage, this bipolar counterpart is both effective and versatile, but the design of the amplifier is more critical to avoid tradeoffs in power. This stage is used in the AD820/822 families.

If a reasonably accurate "pseudo-ground" voltage is required, a voltage-reference IC that can source or sink current is desirable, for example, the AD780 or REF-43 (Figure 1). Operating from a 5-V supply, this circuit handles load currents into/from the 2.5-V source with a low ac impedance, aided by the low ESR bypass caps (either tantalum or aluminum electrolytics). The REF-43 provides a 2.5-V output, as does the AD780, with the same pinout. With pin 8 grounded, the lower-noise AD780 can also be used for a 3-V output; and output transient response can be optimized with optional bypass capacitor, C3.

Other low-voltage references worth considering are standard Zener-like two-terminal types, such as the popular AD589, at 1.235 V, operable over current ranges from 50 μ A to 5 mA. It can be stacked for higher levels in 1.235-V chunks or scaled up by amplification (see below). With two AD589s stacked in a 3-volt application, a 1.235-volt pseudo-ground is inherent.

Power-Supply Conditioning and Noise

Power-supply noise can defeat even the best paper designs if not properly planned for and dealt with. Low-power analog ICs, which tend to have poor supply rejection, are susceptible to the problem. Commonly used 5-V supplies for computer and digital logic circuitry are especially bad (for noise in analog circuitry). Because of both the fast edges inherent in digital circuitry and the prevalent use of switching-type supplies, simple filtering may not be adequate to allow their use with precision analog stages. While use of a supply common to digital circuits may save space and money, its disadvantages should be taken into account where noise is critical.

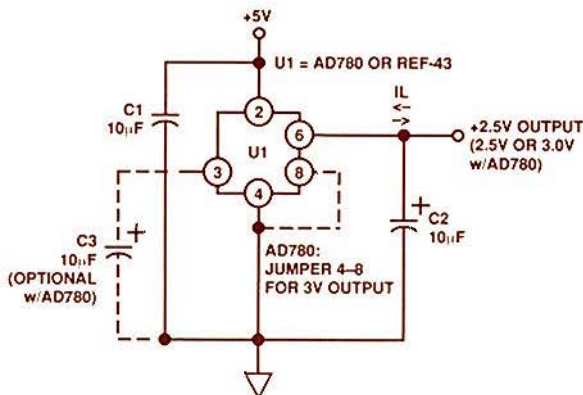


Figure 1. Pseudo-ground at 2.5 or 3.0 V using a reference capable of sourcing and sinking current.

Digital supply feeds taken from the middle of a logic layout contain huge amounts of high frequency noise—100 mV and more. And switching-type logic supplies inherently have large output spikes. It is much better to use a separate, low noise linear-mode supply for sensitive analog circuits where possible.

If a 5-V logic supply must be used, isolation and circuit partitioning can help greatly, as can optimized decoupling and filtering. Make sure that power for analog circuitry is wired directly to the supply terminals, not from downstream logic stages. This avoids both static and dynamic voltage drops due to logic currents and their rapid fluctuations.

Bypass capacitors are usually not by themselves adequate for filtering switch-mode glitches, so additional steps should be taken. For example, one can isolate logic noise with a balanced in-line LC filter^{1, 2}. This filter uses a high-capacitance composite output capacitor and two high-frequency inductors—one in each line—made from a "three-turn" (actually two complete turns) wrapped toroidal ferrite bead. The capacitors, made up of a paralleled 100- μ F electrolytic, 10-to-22- μ F tantalum, and 0.1- μ F ceramic, can be low-ESR switching types for best performance, but this is not absolutely essential. Such filters can suppress logic glitch noise by 40 dB and more.

Watch Out for Circuit-Dependent Swing Limitations

Even if a device has wide output-swing capability, the application configuration can have swing limitations. For example, consider the popular two-op-amp instrumentation amplifier (in-amp) shown in Figure 2; normally a dual-supply design, it is adapted here for single-supply use with selectable gains of 10 \times or 100 \times .

At first glance, one might expect that this 100 \times instrumentation amp should easily amplify small positive voltages, e.g., a +10-mV differential input ($V_{IN(-)} = 0$, $V_{IN(+)} = 10$ mV) to produce +1 V at V_{OUT} . However, even with near-perfect characteristics for amplifiers A and B, closer examination shows a potential difficulty. Note that to satisfy loop requirements and produce 1 V at V_{OUT} , V_{OA} must be 0 V while sinking current, a factor which demands ideal saturation characteristics of U1A. Practically speaking, this in-amp configuration needs excellent output characteristics in both amplifiers for best linearity.

The point is that, even though an op amp may be well-designed for single-supply operation, its performance can still be constrained by the chosen configuration. It's also worth noting that if a 5-resistance in-amp topology is used to obtain single-resistor gain-setting (4 fixed resistances plus a variable gain-setting

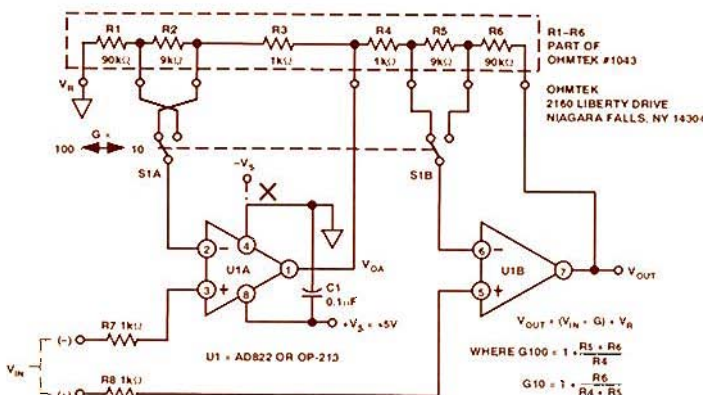


Figure 2. Two-op-amp programmable-gain instrumentation amplifier for single-supply applications.

resistor connected between the summing points), the ideal voltage output demanded of amplifier A can be negative! Thus, although rail-to-rail output-stage op amps help improve CM handling (see sidebar), topology is also important to performance.

In spite of these inherent limitations, the topology of Figure 2 is still very useful when carefully applied. For gain of 100, the circuit provides subtraction with gain (and common-mode rejection) when the two ratios, $(R_1 + R_2)/R_3$ and $(R_5 + R_6)/R_4$, are equal. The $100\times$ gain ($G = 100$) is equal to $1 + (R_5 + R_6)/R_4$. In the switch's gain-of-10-position, the gain is $1 + R_6/(R_5 + R_4)$. For either gain, the resistor ratios on both sides must be equal for good CMR.

This approach has advantages and disadvantages in practical implementation. It is not as simple in concept to gain-program as the 5-resistor topology (which simply adds an R_G resistor between the summing points of a 4-resistor ratio-matched network). However, it's worth noting that, in the topology of Figure 2, 10-to-100 Ω of series switch resistance has negligible effect on gain accuracy, while it would have significant impact when switching R_G in the five-resistance topology.

Keys to performance of this circuit are the resistor network and the amplifier. For best performance with premium amplifiers, the network should have a ratio-match specification of 0.1% minimum, and 0.01% as a goal. For ideal amplifiers, the output CM error due to 0.01% match resistors will be of the order of -100 dB for a gain of 10, or -120 dB for a gain of 100. The suggested network is available with ratio-matching to 0.01%.

The circuit can be easily gain-switched with jumpers, or CMOS switches, e.g., a 3.3- and 5-volt-specified DPDT ADG513 quad switch, used as shown. Operating on single supplies, the CM limitations of the configuration must be observed, as noted. V_{OUT} will be referred to the potential applied to the network's V_R pin (but watch out for potential difficulties due to inverted V_R on the

intermediate output, V_{OA} ; $V_{IN}(-)$ must be more positive than V_R). With dual supplies ($-V_S$ connected as noted), these caveats are eased.

Suggested amplifiers for U1 are either the AD822 or an OP-213, depending on source resistances at V_{IN} . The AD822 is available with offset as low as 0.4 mV and typical drift of $2 \mu\text{V}/^\circ\text{C}$; it is well suited to high impedances calling for very low bias currents, a circumstance found in bio-medical applications, high-Z bridges, etc. The OP-213, with its offset of 150 μV and typical drift of $0.2 \mu\text{V}/^\circ\text{C}$, will be better suited to those uses requiring lowest noise and/or drift—especially at high gains—such as load cells.

Look for Devices Designed for Single-Supply Use

The discussions above should make one general point clear: for designs requiring single supplies, it is usually most fruitful to employ amplifiers expressly designed for the job. Among the performance specs that will be enhanced are supply power and operating ranges, dynamic range, input/output ranges, and increased overall linearity. In addition to the sampling of newer op amp types (Table 1), there are other IC devices designed for single-supply/low power operation.

We've briefly discussed references here, mentioned the ADG511/12/13 switch series, and considered the design of high-input-impedance instrumentation amplifiers for single supplies. Although endowed with somewhat lower input impedances, the AMP-04 single-supply in-amp (*Analog Dialogue* 27-1) and the AD626 low-cost single-supply (+2.4 to +10-V) differential amplifier, with fixed gains of 10 and 100 (*A-D* 26-1), are worthy of mention. Tables 2 and 3 illustrate typical characteristics of general-purpose Analog Devices single-supply ADCs and DACs that are specified to operate on +5-V single supplies. While space does not permit detailed discussion of their performance, these data can serve as an introduction to what is available for systems employing A/D and D/A conversion.

Table 2. A/D Converter Chips Compatible with Single-Supply Systems

Device	Resolution (Bits)	Multiplex Capability (Channels)	Supply Voltage (V)	Input Range 0 to (V) or (\pm V)	Output Format Ser/Par	Reference Ext/Int (V)	Architecture Type	Conversion Speed ksp/s
ON-CHIP SAMPLING								
AD7575	8	1	5	2.46	Parallel ⁽⁴⁾	Ext 1.23	Successive apx	200
AD7820	8	1	5	5	Parallel ⁽⁴⁾	Ext	Half-flash	500
AD7821	8	1	5 ⁽¹⁾	5, ± 5	Parallel ⁽⁴⁾	Ext	Half-flash	1000
AD7824/28	8	4/8	5	5	Parallel ⁽⁴⁾	Ext	Half-flash	400
AD7579/80	10	1	5	2.5, 5, ± 2.5	Parallel ⁽⁴⁾	Ext 2.5	Successive apx	50
AD7776	10	1	5 ⁽¹⁾	2	Parallel	Ext/Int	Successive apx	400
AD7777	10	4	5 ⁽¹⁾	2	Parallel	Ext/Int	Successive apx	400
AD7778	10	8	5 ⁽¹⁾	2	Parallel	Ext/Int	Successive apx	400
AD7880	12	1	5 ⁽⁵⁾	5, 10, ± 5	Parallel	Ext	Successive apx	66
AD7883	12	1	3 ⁽⁵⁾	3, 6, ± 3	Parallel	Ext	Successive apx	50
AD7890-x ⁽²⁾	12	8	5	2.5 ⁽²⁾	Serial	Ext/Int	Successive apx	100
AD7893-x ⁽³⁾	12	1	5	2.5 ⁽³⁾	Serial	Ext 2.5	Successive apx	117
AD7710/11/12/13	24	1-3 ⁽⁶⁾	5 ⁽¹⁾	0.02, 2.5	Serial	Int	Charge-bal ⁽⁷⁾	Filter-dep.
OFF-CHIP SAMPLING								
AD670	8	1	5	0.255, 2.55	Parallel ⁽⁴⁾	Int	Successive apx	10 μs
AD875	10	1	5 ⁽⁵⁾	2 V p-p	Parallel ⁽⁴⁾	Ext 2.0	Pipelined flash	15000
AD776	16	1	5	4	Serial	Ext/Int	Sigma-delta	100

NOTES

¹Operates with wider (or dual) supply range also.

²Input range is 0 to 2.5 V for AD7890-2, 0 to 4.096 V for AD7890-4, ± 10 V for AD7890-10.

³Input range is 0 to 2.5 V for AD7893-2, 0 to 5 V for AD7893-5, ± 10 V for AD7893-10.

⁴Three-state output interface.

⁵Power-down function available.

⁶On-chip programmable-gain amplifier, $G = 1$ to 128.

⁷On-chip microcontroller, auto-zero and auto-cal functions.

SINGLE-SUPPLY CIRCUIT APPLICATIONS

Some selected applications illustrate the general design concepts discussed above.

References for Low Power Systems

There are a variety of considerations when stable, accurate dc voltage references are made to work from 5 V (and lower) supplies. These include: quiescent power consumption and overall power efficiency, the ability to operate down to 3 V, low input/output (dropout) capability, and minimizing noise output. Because supplies less than 5 V can't support devices such as buried Zener diodes, low voltage references must necessarily be bandgap types. Figure 3 and 4 show reference circuits that can work at >3 V.

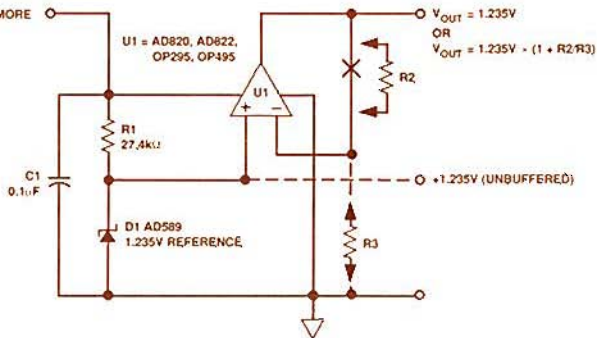


Figure 3. Buffered reference for 1.23 V or more, using a supply voltage ≥ 3 V.

It is difficult to get a reference to work well down to 3 V, a condition that dictates use of a lower-voltage reference diode. A solution is a two-terminal (hence "diode") 1.235-V reference based on a bandgap circuit, and appropriate low-power support circuitry, as shown in Figure 3.

Table 3. D/A converter chips compatible with single-supply systems

Device	Resolu- tion (Bits)	DACs (Channels)	Supply Voltage (V)	Output Range 0 to (V) or (V=V)	Output Format ⁽¹⁾	Reference
AD557	8	1	5	2.56	Parallel	Internal
AD558	8	1	5 to 15	2.56, 10	Parallel	Internal
PM1-7528	8	2	5 ⁽¹⁾	1.23 ⁽²⁾	Parallel	External 1,2,3
DAC-8408	8	4	5	1.23	Parallel ⁽³⁾	External 1,2,3
PM1-7226A	8	4	5 ⁽¹⁾	1.23	Parallel	External 1,2,3
AD7225A	8	8	5 ⁽¹⁾	1.23	Parallel	External 1,2,3
DAC-8841	8	8	5	3	Serial ⁽⁴⁾	External 1,5
ADV7128	10	1	5	0-17.61 mA ⁽⁴⁾	Parallel	External 1,2,3
DAC-8512	12	1	5 ⁽¹⁾	4.095	Serial ⁽⁴⁾	Internal
DAC-8562	12	1	5 ⁽¹⁾	4.095	Parallel	Internal
DAC-8221	12	2	5 ⁽¹⁾	1.23 ⁽²⁾	Parallel	External 1,2,3
DAC-8222	12	2	5 ⁽¹⁾	1.23 ⁽²⁾	Parallel	External 1,2,3
DAC-8248	12	2	5 ⁽¹⁾	1.23 ⁽²⁾	Parallel	External 1,2,3
DAC-8412/13	12	4	5 ⁽¹⁾	2.5	Parallel ⁽³⁾	External 2,5
DAC-8420	12	4	5 ⁽¹⁾	2.5	Serial	External 2,5
AD1866	16	2	5	2.5=1	Serial	Internal
AD1868	18	2	5	2.5=1	Serial	Internal

NOTES

- ¹Operates with wider supply range also.
- ²Unbuffered analog output (≈ 11 k Ω).
- ³Read/write parallel interface.
- ⁴Three-wire serial interface.
- ⁵Internally latched.
- ⁶Video level of 0.6 V into 37.5 Ω (75 Ω double-terminated).

The low-current diode used for D1 is the 1.235 V AD589. Resistance R_1 sets the current, chosen for the device's minimum specified current, 50 μ A (5-mA max), at a minimum supply of 2.7 V. At this low value of current, loading on the unbuffered diode must also be minimized, but generally static loads of a few μ A are all right (if accounted for). The dynamic impedance of the diode decreases to about 1 ohm with 500 μ A.

Amplifier U1 buffers and scales the 1.235-V reference, so that higher source or sink load currents can be handled. The cost is 150 μ A of quiescent current through U1, using one channel of an OP-295, or 700 μ A using an AD820. Without gain scaling resistances, R_2 - R_3 , the output is simply 1.235 V; with these resistors, the output can be set anywhere between the supply rails, due to the specified device's rail-to-rail range. This buffered reference is inherently "low dropout"—furnishing a +4.5-V reference output on a +5-V supply, for example.

Noise output will be dominated by the diode's ≈ 100 to 200 nV/ $\sqrt{\text{Hz}}$, but this can be filtered (as the next circuit shows); with an AD820 one achieves lowest overall noise and substantial drive current (15 mA).

Amplifier standby current can be optionally reduced to 20 μ A if an OP-90 is used, and all devices mentioned operate from supplies as low as 3 V. Output voltage drift, primarily a function of the diode grade, can be as low as 10 ppm/ $^{\circ}$ C.

Low-Dropout Regulators

With a boost transistor added within a low-dropout reference circuit, output currents >100 mA are possible, while still retaining low standby current and low dropout voltage.

Figure 4 shows a low-dropout regulator with 800 μ A of standby current, suitable for a variety of voltages and output currents up to 100 mA. It achieves a 100-mA current using a controlled-gain pass transistor, Q1, an MJE170 type. Output current control is provided by limiting base drive to Q1 by a series resistance, R_3 . This limits the base current to about 2 mA, so that with maximum HFE of Q1, no more than 500 mA is allowed to flow, limiting short-circuit dissipation to safe levels (if a heat-sink and fuse are employed).

Output voltage level is chosen simply by programming R_1 , according to the table. Dropout with a 100-mA load is about 200 mV; thus a 5-V output is maintained for inputs above 5.2 V (see table). Output voltages down to 3 V or less are possible.

The circuit responds well to stepped loads; transient error is only a few mV, p-p, for a 30-100-mA load change. This is achieved

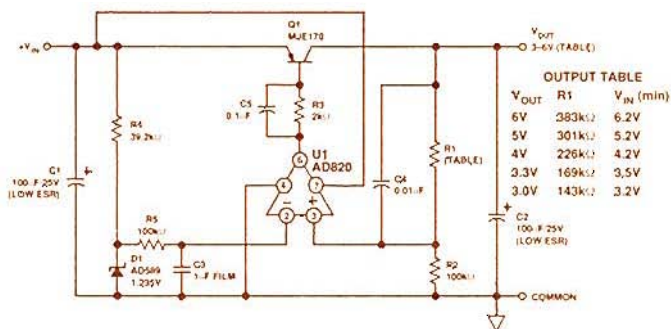


Figure 4. Low-dropout, low-noise, low-voltage regulator capable of 100-mA output.

partially through the use of low ESR switching type capacitors (C_1 - C_2); the circuit also works with smaller value conventional electrolytics (but with greater errors).

Low output noise is attained in this circuit with the reference filter, R_5 - C_3 . An OP-295 can be used as the amplifier; it allows lower overall standby current ($\approx 200 \mu\text{A}$), but has greater transient errors due to reduced bandwidth.

4-20 mA Loop Circuits

Amplifier devices with outputs that swing close to the negative rail enhance and/or simplify 4-20-mA loop transmitter designs, as exemplified in Figure 5. In this loop-powered strain-gage sensor application, a 50-mV full-scale (FS) bridge output is amplified and calibrated for a 4-20-mA transmitter output. Power is furnished by the remote loop supply of 12 to 36 V.

U1, an AMP-04 single-supply in-amp, amplifies the bridge signal with a gain of about 40 V/V; [$G = 100,000/R_G$]. The AMP-04's output range includes the negative rail, so a 0 to 50-mV bridge signal is amplified to 0 to 2.01 V, referred to the common bus (U1, pin 5). With all the devices' negative supply pins referred to this bus, the bulk of the loop quiescent current flows through R_6 , the external loop, and termination, R_{LOAD} .

U2 acts as a summing V-to-I converter, which produces an output span of 0 to 16 mA, proportional to the bridge output signal. In addition, since the total quiescent current of the circuit adds up to something less than 4 mA, U2 produces an incremental reference offset to bring the minimum loop current up to 4 mA. The signal and reference voltages are converted to currents, which are summed and flow through R_5 . The output of operational amplifier, U2, drives pass transistor, Q1, to produce a current flowing through R_6 such that its voltage drop must equal that in R_5 , in order to maintain the summing point, pin 3 of U2, at a null.

With zero bridge output, U1's output will be at the negative rail. No current flows into the summing point of U2 via R_1 - R_2 , since the summing point is at this same potential. For this zero-signal condition, the loop is calibrated via R_3 (NULL, or reference) to produce a 4-mA output current, or 0.4 V across a 100- Ω R_{LOAD} . With zero current through SPAN adjustment, R_1 , the 4 mA can be set independently. The NULL-SPAN trims are inherently non-interactive because of the null at the summing point of U2.

R_3 and R_4 , connected between the output of 5-volt-reference U3 and the summing point's virtual ground, produce the constant

incremental reference current, which is scaled by the loop current-gain resistors, R_5 and R_6 . This current, I_{NULL} , is:

$$I_{NULL} \approx \left[\frac{5 \text{ V}}{R_3 + R_4} \right] \left[1 + \frac{R_5}{R_6} \right]$$

where 5 V is the output of reference U3, which is driven by the remote loop supply. R_3 is adjusted to set I_{NULL} for 4-mA loop current.

The bridge output is amplified (to 2.01-V for 50-mV bridge output) by U1, and converted to signal current to the U2 summing point by R_1 and R_2 . There it is summed with the incremental reference current, and amplified by R_5 and R_6 . Its contribution, I_{SPAN} , is:

$$I_{SPAN} \approx \left[\frac{G V_{BRIDGE}}{R_1 + R_2} \right] \left[1 + \frac{R_5}{R_6} \right]$$

where V_{BRIDGE} is the output of the bridge, and G the AMP-04's gain. Full-scale current output is trimmed by adjusting R_1 (SPAN), with a 50-mV FS bridge output, for 20-mA output current (4-mA quiescent-current-plus- I_{NULL} plus 16-mA I_{SPAN}), or 2 V across R_{LOAD} .

In this circuit the three active devices and the 3500- Ω bridge consume 3.75 mA maximum, less than the system's 4-mA reference level, so some NULL current is always needed. C_1 provides 7-Hz low-pass filtering, to limit noise, while C_2 stabilizes the U2 output loop. The 0-to-16-mA I_{SPAN} portion of the loop output, plus the NULL current, is passed by Q1 (TO-220 package).

5-V Single-Supply D/A Converters

At present, most of the available DACs (D/A converters) require dual power supplies. For those that don't, supplies of 12-to-15 V are usually required. At the moment, this factor limits DAC choices for use with single +5-V supply system power.

CMOS R-2R ladder DACs are a natural choice for low-power operation; and many of these units are designed to work on 5 V supplies. However, if used in the standard multiplying mode they also require a negative supply for the inverting output amplifier, and they require a negative reference for positive output (or vice versa). In order to make such a DAC operate on a single polarity, it can be turned around and operated in what is known as its inverted, or voltage output mode. Most CMOS R-2R DACs can operate in this fashion, even if not specified to do so^{3,4} (see Table 3, again).

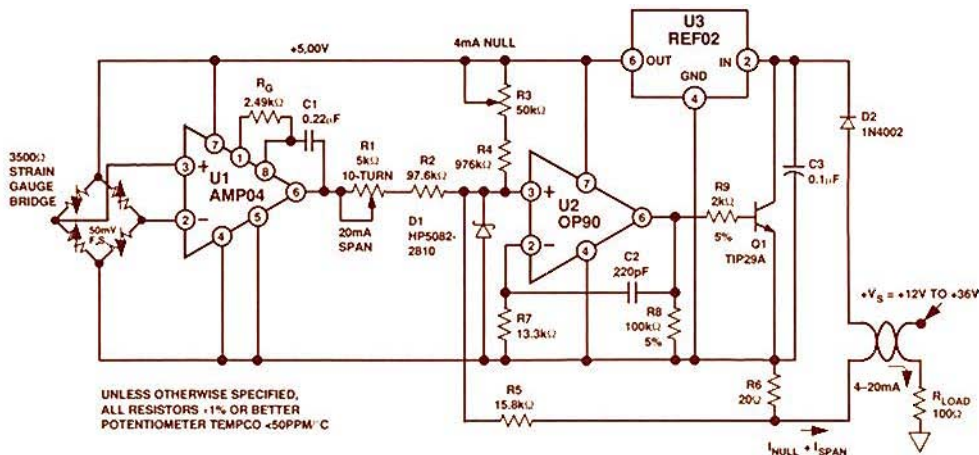


Figure 5. Precision bridge-output-to-4-20-mA-loop transmitter with non-interactive trims deriving all excitation functions from loop supply.

Using a 12 bit DAC-8043 in this mode with the pinout shown in Figure 6, the ladder input labeled V_{REF} becomes the voltage output node (pin 1), and the normally I_{OUT} node becomes the reference input (pin 3). This voltage-mode CMOS DAC circuit, using two 8-pin ICs and interfacing serially, works on a single 5 V supply; it is scaled for 0-to-4.095-V output range (or 1 mV/LSB).

The circuit is clean and straightforward, but some practical points are worth noting to obtain best results. With a 5-volt supply, the internal NMOS switches have only $[5\text{ V} - V_{REF}]$ as enhancement voltage, or 3.765 V with a 1.235-V reference. This is about as high a reference voltage as one should apply to the DAC operating in this fashion. If higher V_{REF} values are used, the MOSFET gate drive can become starved, resulting in higher On resistance and nonlinear output voltage.

This circuit uses an DAC-8043, a 12-bit multiplying DAC, so the output voltage will be $[D/4096] \cdot V_{REF}$, where "D" is the numerical value of a 12 bit digital word—ranging from 0-4095. With $V_{REF} = 1.235\text{ V}$, the unbuffered output at pin 1 of U1 is $[4095/4096] \cdot 1.235\text{ V}$ at all-1s, or [full-scale - 1 LSB].

The output amplifier, U2, amplifies the voltage at the DAC output by the gain value, G , to meet the needs at its destination. The resistance values are chosen here to provide a scale factor of 1 mV/LSB with an appropriate adjustment of R_4 . The gain required of U2 for this weighing is about 3.3, and is made variable to trim out tolerances in both the reference voltage and gain resistors. Also, to balance out voltage offsets due to bias current (for amplifiers where this is a consideration), the values chosen help to make the equivalent resistance of the gain divider equal to the DAC output resistance, $\approx 11\text{ k}\Omega$.

For a linear V_{OUT} range of 0 to 4.095 V, the amplifier must be capable of rail-to-rail output, for example, the OP-295 or the AD820 (AD822). DC accuracy, speed, and power are strongly affected by the choice of U2, and some tradeoffs may be necessary for the best overall choice. Relatively slow response and best overall DC accuracy is possible with the OP-295—or faster response with good, but somewhat reduced, accuracy using the AD820. The OP-295 has a max V_{OS} of 300 μV , so worst-case output offset is about 1 mV; with the AD820B this increases by a factor of 1.3 (and can be optionally nulled).

Both amplifiers can source a 4.095-V output, using a 4.75-V supply, with the AD820 capable of 10 mA, the OP-295, 5 mA. The rail-to-rail output stages of both allow linear swings close to

ground. For the OP-295, the CMOS output stage allows linear outputs to within $\leq 1\text{ mV}$ of ground, while the bipolar output of the AD820 pulls down to about +5 mV.

Settling time using the OP-295 is below 150 μs , but the AD820 can improve it to about 2.5 μs , due to the higher slew rate. The tradeoff here is power; one channel of an OP-295 with the DAC consumes about 660 μA , while the faster AD820 uses $\approx 1.2\text{ mA}$.

Complete, single IC buffered 12 bit single-supply DACs are also available, and the function just described can be realized in both serial and parallel input formats with the DAC-8512 and DAC-8562, respectively, as noted in Table 3.

Precision Temperature Sensing

Many methods of sensing temperature are available, but very high precision on single power supplies remains a challenge. Figure 7 shows how a precision platinum resistance-temperature-device (RTD) sensor circuit can be implemented on 5 V. The RTD bridge is driven with a regulated 200- μA current, I_{BRIDGE} , minimizing self-heating. Overall current drain is 1.3 mA, and the circuit works from supplies of 5 V for a 0-400°C output, or as little as 4.5 V for 0-350°C.

The 200- μA current is sensed by R_{SENSE} , and the voltage it develops across the 1-k Ω resistor is compared to a 0.2-V reference appearing across R_5 in the U1-A control amplifier—an OP-295, which allows input voltages of 0.2 V. The rail-to-rail output provides ample bridge-drive headroom. At the bridge output the common-mode voltage is 0.21 V, a difficult-to-handle level for conventional 5-V in-amps, IC or discrete. In this circuit the output is amplified by U3, an AMP-04.

This device has an input CM range of 0-3.5 V and an output range of 0 to 4.2 V, operating on 5 V. The AMP-04 gain with the value of R_{GAIN} shown here is nominally 245, and this gain times the bridge output voltage of 38 $\mu\text{V}/^\circ\text{C}$ yields a V_{OUT} sensitivity of 10 mV/ $^\circ\text{C}$. C_1 provides a low-pass filter function in conjunction with a 100-k Ω resistor inside the AMP-04, with 3.4-Hz cutoff.

Several factors concerning the surrounding circuit are important for best performance. All critical resistors(*) should be 0.5%, $\pm 25\text{ ppm}/^\circ\text{C}$ types, or about 100 times better than the RTD's temperature coefficient (TC) of 3850 ppm/ $^\circ\text{C}$. R_1 - R_3 , in particular, should be same-manufacturer/same-batch units, with R_4 by the same manufacturer (all of which helps minimize differential TCs. Gain resistance, R_8 , should have a TC low with respect to

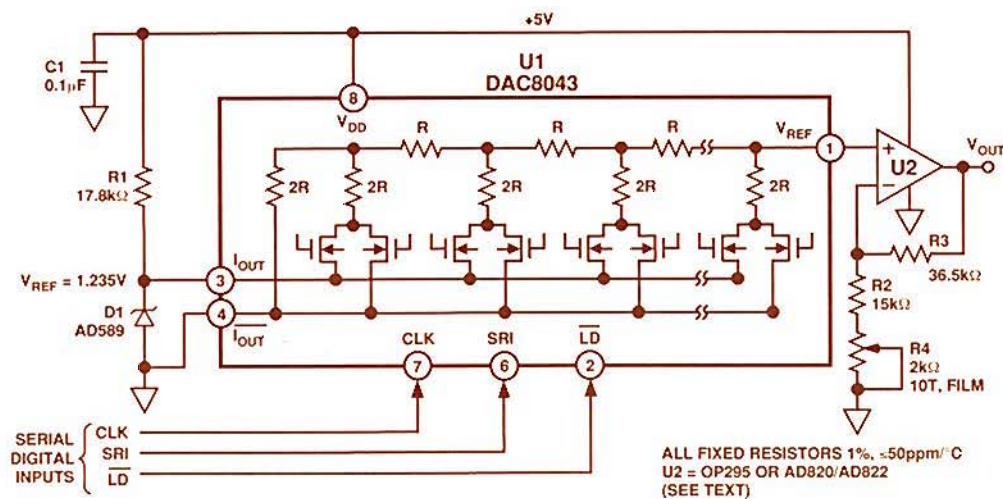


Figure 6. 12-bit DAC with rail-to-rail output buffer for single +5-V supply.

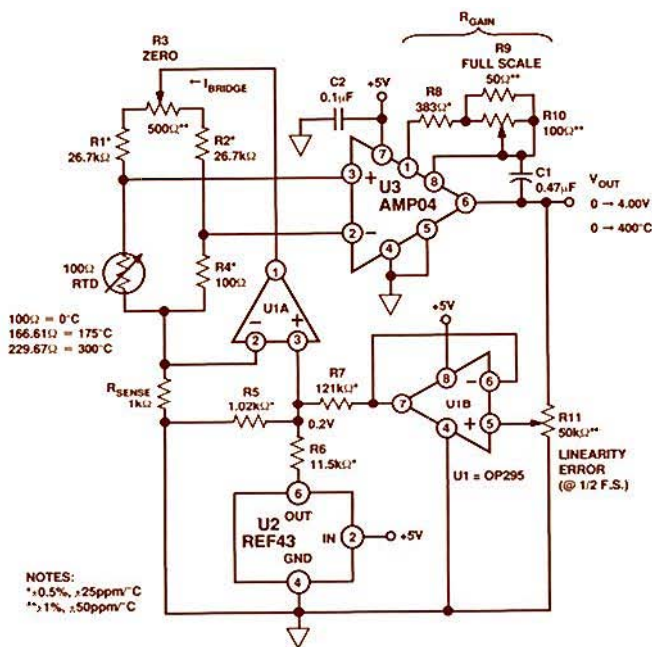


Figure 7. Precision single-supply RTD bridge and amplifier with feedback linearization.

the AMP-04's TC (50 ppm/°C). Less-critical resistors (**) with smaller percentage-error contributions can be more loosely controlled. All trimmers should be multiple-turn film types.

The bridge/amplifier combination has a small amount of non-linearity, typically $\leq 0.5\%$. In comparison, the RTD has a much larger non-linearity, as much as 6°C over a 400°C span, or 1.5%. Fortunately, this non-linearity can be corrected with controlled positive feedback, increasing bridge drive with increasing output. A fraction of V_{OUT} is picked off by R_{11} , buffered by U1-B, and summed with the reference voltage via R_7 . With correct adjustment, this cancels the RTD non-linearity.

Calibration is a relatively simple 3-step process. First, care must be taken in setting for 0°C, since the lack of a negative supply prevents this end point from attaining 0 V. One technique (step 1) is to substitute a resistance of exactly 100 Ω for the RTD (or place the actual RTD in an ice bath solution), and adjust R_3 (ZERO) until V_{OUT} begins to swing positive. Then, trim R_3 in the reverse direction until V_{OUT} just stops changing, which should be at 0 V.

For the FULL-SCALE trim (step 2), preset R_{11} to a midpoint and substitute a 274.04-Ω resistor for the RTD. Then trim R_9 for 4.000 V at V_{OUT} (400°C). For LINEARITY (step 3), substitute a 175.84-Ω resistor for the RTD, and trim R_{11} for 2.000 V at V_{OUT} . Steps 2 and 3 should be repeated for best accuracy, as they interact. When fully trimmed, the output errors of the circuit are within $\pm 0.5^\circ\text{C}$ over the 0 to 400°C range

Single-Ended High-Impedance Microphone Preamp

The microphone preamplifier is a basic audio low-level circuit. While it can assume a variety of forms, designs for low-voltage, single-supply systems can be particularly challenging, because there are few devices with really low noise on 5-V power. The choice gets easier if the total supply voltage is ≥ 10 V, or if a higher-voltage dual supply can be used.

Figure 8 shows a simple non-inverting stage with a single-ended input, a useful approach with high-impedance microphones—higher-Z dynamic types and crystal or ceramic piezoelectrics. The

circuit, with a gain range of 20-40 dB, can be readily optimized for microphones with impedances ≥ 600 Ω. The op amp used for U1 affects performance in general and suitability for single-supply operation. U1 should preferably have low input noise with ≥ 500 -Ω sources. The most suitable types are the AD820, and the dual SSM-2135 and AD822.

Gain-determining resistors, R_1 and R_2 , are scaled for parallel resistance less than the expected source impedance, to minimize their noise contribution at high gain. Gain is adjusted with R_2 , while capacitors C_1 , C_2 , and C_3 decouple dc levels. The amplifier biasing and resistors must not introduce noise, even indirectly⁵; thus, resistors with dc across them (R_1 , R_3 , R_7 , and R_8), and the gain resistors, should have low excess noise—metal films are preferred—or be bypassed (R_7 , R_8). R_7 - R_8 bias the U1 output to 2.2 V (in this case) for maximum symmetrical output swing.

While the SSM-2135 is optimum when operating from low-impedance sources, the FET-input AD820 (or AD822) is preferable with high-impedance crystal or ceramic mikes. For such sources, R_3 and R_4 should be 1 MΩ or more, with C_1 a 0.1-μF film capacitor. The input cable to the microphone must be short and shielded. With symmetric dual supplies, R_3 is grounded and $-V_S$ is applied to U1; Xs mark the spots.

Bandwidth at maximum gain is about 30 kHz with the SSM-2135, 20 kHz with AD820. With a shorted input, the SSM-2135 measures an output noise of about 110 μV rms at a gain of 100, and 0.022% 1-kHz THD+N with 1 V rms into a 2-kΩ load. Similar tests with the AD820 give about 200 μV rms and 0.05% THD+N. All figures improve at lower gains. ▶

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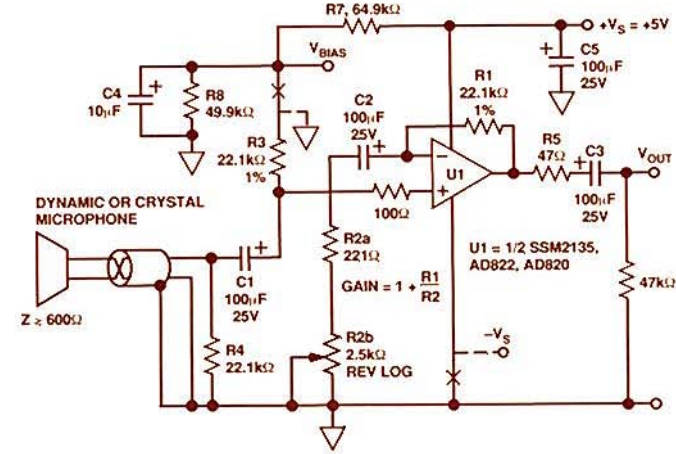


Figure 8. Single-ended, single-supply, high-impedance microphone preamplifier is useful with various microphone types.

What's New in DSP

Fast 3-Volt Digital Signal Processor

ADSP-2103 is pin- and code-compatible with ADSP-2101, Dissipates 65 mW maximum, 10 mW in standby

The ADSP-2103, the first of a series of 3 volt-powered digital signal processors (DSPs), is a 16-bit fixed-point unit, functionally equivalent to the industry-standard ADSP-2101. Using transistor-size reduction and design enhancements, it maintains 13-MHz performance, dissipating 30 mW in typical operation, 65 mW maximum, and less than 10 mW in a software-controlled "idle" mode.

The ADSP-2103 is ideally suited for DSP and mixed-signal applications that demand high performance, low power drain, and increased battery life, e.g., such portable equipment as GSM, TIA, CT2, and other handheld cellular telephones, laptop and notebook PC modems, remote instrumentation, and data loggers.

Based on the ADSP-21xx processor core, (like the ADSP-2101), it includes 2K words of program-memory RAM, 1K



words of data-memory RAM, two serial ports and an interval timer. It operates at 3.3 V ($\pm 10\%$), with maximum power dissipation of 65 mW at 13-MHz clock (compared to the ADSP-2101's 275 mW). It is supported by the standard set of ADSP-21xx software development tools and uses the same object code files as the ADSP-2101. It is available in PLCC and PQFP packages at comparable prices to the ADSP-2101. Circle 7

...and even more briefly:

Personal sound architecture for PCs, Modem datapump chipsets, Signal port for PSTN

Personal Sound Architecture (PSA) is a programmable architecture for flexibly integrating sound into personal computer systems. Cards based on chip sets comprising DSPs (like the ADSP-2115), codecs (like the AD1848), and interface chips (like the ECHO® ESC614) are developing widespread support for use in software-defined applications, such as music synthesis, audio compression, and spatial effects at low cost.

Such products are compatible with standard applications, looking in both directions—for example, emulating Sound Blaster®, compatibly with the installed base of games; on the other hand, compatible with Microsoft Windows Sound System™. Circle 9

An example is the low-cost Cardinal "Digital Sound Pro 16" audio card, widely available at retail in the U.S.—and on its way to store shelves worldwide. It claims



0.012% harmonic distortion, 84.8-dB SNR, 67.5-dB stereo-channel separation, and ± 3 dB bandwidth, 20 Hz to 20 kHz.

Datapump chipsets: These chipsets, comprising an ADSP-21xx processor, an AD28msp01 signal port for PSTN (public-service telephone network) applications, and an interface chip, use Digicom Systems datapump algorithm software to implement high-performance modems at low cost. Circle 10

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M-S Processors

Include DSP, memory, plus On-chip 16-bit ADC & DAC

The ADSP-21msp50A/55A/56A are high-performance fully integrated systems on a chip, based on the mixed-signal-processor architecture introduced earlier in these pages (*Analog Dialogue* 24-2, 1990, pp. 3-7). They combine, on a monolithic CMOS chip, a 13-MHz general-purpose signal-processing core like that of the ADSP-2111, a 16-bit ADC, 16-bit DAC, and signal-conditioning circuitry.

The ADSP-21msp5x processor family provide a low-cost and compact means of processing voice-band analog signals in applications such as digital mobile radio, analog cellular radio, personal computers, telephone answering machines, voice-mail systems, pagers, and personal assistants, especially where separate DSP and codec components are not feasible.

These processors are fully code-compatible with all other members of the ADSP-21xx family of 16-bit fixed-point DSPs, and every instruction is executed within a single clock cycle. In addition to the base architecture (3 computational units, 2 data-address generators, and a program sequencer), the chip has a host interface port (HIP), programmable timer, and extensive interrupt capabilities.

All three devices include 2K words of on-chip program-memory RAM and 1K word of on-chip data-memory RAM. In addition, the ADSP-21msp56A contains 2K 24-bit words of on-chip program-memory ROM.

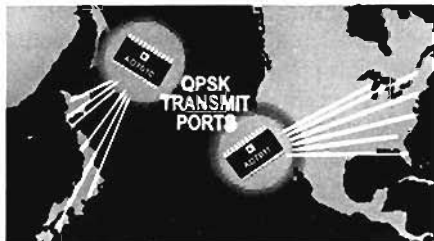
The high-performance analog interface has 65-dB S/(N+D), useful in high-quality speech-processing, and includes programmable gain stages and on-chip anti-aliasing and anti-imaging filters, in addition to the 16-bit ADC and DAC. To conserve energy in battery-powered equipment, a <1-mW power-down mode is provided, with 100-cycle recovery.

The '50A is packaged in a 144-pin PGA; the more-compact '55A and '56A come in low-profile 100-pin PQFP's. Prices start at \$45 in 1000s. Circle 8

Chips for communications: Ports, PLLs, Synthesizers

QPSK Transmit Ports

AD7011 for North America
AD7010 for Japan JDC



The AD7010 and AD7011 are QPSK Transmit ports for digital communications. They generate quadrature differential $\pi/4$ QPSK-modulated signals, derived from a serial data stream. The AD7011's output is specified for operation in North American IS-54 digital cellular phones, while the AD7010 meets the Japan Digital Telephone (JDC) standard. Both include ROM lookup table, a pair of 10-bit pulse-shaping DACs, and a pair of Bessel filters for DAC image attenuation.

Features include differential outputs, on-chip reference, and signal power ramping. Operating on a single +5-V supply from -40 to $+85^\circ\text{C}$, they are housed in a 24-pin shrink small-outline package (SSOP)—50% smaller than SOIC). Prices (1000s) are \$6.30 and \$9.37. Circle 12

General-Purpose I/O Port Includes auxiliary DAC port

The AD7001 is a complete I/O port. A critical building block of digital cellular GSM phones, the AD7001 converts two channels of digitally modulated Transmit data into a pair of analog outputs. On-board anti-imaging filters insure excellent rejection of DAC-generated images. The Receive path consists of fixed and programmable analog gain blocks, followed by a 2.16-Msps 8-bit A/D converter. The wide input bandwidth of the ADC makes it suitable for use in GSM digital mobile telephony.

Features include on-board reference and power-down modes. Operating from -25 to $+85^\circ\text{C}$, it is housed in a 44-pin PQFP. Price in 100s is \$26. Circle 13

Monolithic Direct Digital Synthesizer

AD7008 clocks at up to 50 MHz, includes 10-bit DAC
Has 32-bit frequency resolution, 12-bit phase resolution

The AD7008 is a monolithic direct digital synthesizer with analog output provided by an on-chip 10-bit current-output D/A converter. Included on chip are a 32-bit phase accumulator, sine and cosine lookup tables, a 1.27-V reference, and modulation facilities for phase modulation, frequency modulation, and both in-phase and quadrature AM—suitable for single-sideband generation.

Powered by a single +5-volt supply, the CMOS chip can be clocked at rates up to 20 and 50 MHz (AD7008AP20 and AD7008JP50). With a 50-MHz clock, it can generate usable output frequencies up to 20 MHz. The modulation signal registers may be loaded through either parallel or serial interfaces, and a frequency-select pin permits selection between two frequencies on each cycle.

The AD7008 can be used in a variety of

applications. Its primary use is in the generation of fast frequency-hopping local-oscillator signals required in modern analog and digital land mobile radios. Its modulation capabilities make it especially suitable for applications requiring direct generation of modulated IF signals from a digital source. Other applications include satellite receivers, imaging, wireless base stations, and test instrumentation.

Specifications include 50-dB minimum SNR at the maximum clock rate and -55 -dB max THD at 20 MHz while generating a 2-MHz sine. Full-scale output is 1 V into a 50-ohm load.

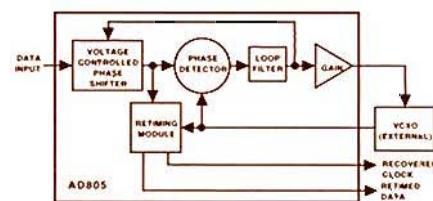
The AD7008 is available in two versions, for 20-MHz (-40 to $+85^\circ\text{C}$) and 50-MHz (0 to $+70^\circ\text{C}$). Both versions are packaged in a 44-pin PLCC. Prices (1000s) start at \$22.50. Circle 14

Data-Retiming Phase-Locked Loop

AD805 provides 155-Mbps clock recovery & data retiming
Exhibits no pattern jitter; Random jitter $<1^\circ$ rms

The AD805 is a data retiming phase-locked loop designed to perform clock recovery and data retiming on non-return-to-zero (NRZ) data at 155.52 megabits per second. Its primary application is in SONET (synchronous optical network)/SDH (synchronous digital hierarchy) fiberoptic regenerative applications. For excitation, it uses a single -5.2 -V (or $+5$ -V) supply and an external voltage-controlled crystal oscillator (VCXO), for example, the Vectron CO-434Y Series.

The AD805 meets or exceeds CCITT regenerator specifications G.958 for STM-1 Type A (resonant filter) wideband jitter tolerance and Type B (phase-locked loop) narrow-band jitter transfer. This means that accumulated jitter over many stages of signal regeneration in fiberoptic systems stops at the AD805; it will not add excessive jitter of its own. In addition, the AD805 has no problem with Type A & B regenerators "intervorking".



Acquisition time is less than 44 bit periods for a 2^7-1 pseudo-random number (PRN) sequence, and random jitter is less than 1° rms for both 2^7-1 and $2^{23}-1$ PRN sequences. The AD805 virtually eliminates pattern jitter, and there is fundamentally no jitter peaking. NRZ data does not require a preamble, and up to 500 bit-periods of transitionless data will be passed without error. The AD805 is compatible with 10 KHz ECL data. It is packaged in a 20-pin plastic DIP and operates from -40 to $+85^\circ\text{C}$. Price in 100s is \$45.70. Circle 15

Sampling ADCs for Size, Channels, Resolution

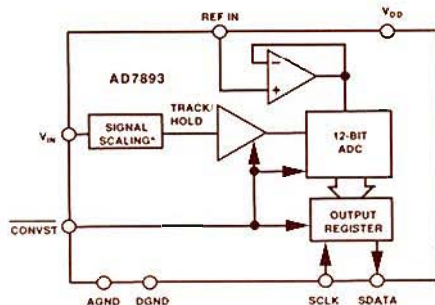
Single-Supply 12-Bit ADC with 8 Pins

AD7893 operates from +5 V, dissipates 45 mW
Serial interface, throughput rates up to 117 kps

The AD7893 is a fast 12-bit sampling A/D converter, available in 8-pin miniDIP and low-profile (0.15"–3.81 mm) SOIC packages. Operating from a single 5-volt supply, it has low power dissipation, 45 mW, max, and a throughput rate of up to 117 kps. Communication is serial, via a high-speed, 2-wire-plus-ground interface.

The AD7893 needs only a 2.5-V reference input and decoupling capacitors to form a complete single-channel data-acquisition system. The reference may be derived from the power supply, from an accurate low-ppm external reference; or from the same reference as the input source for ratiometric operation.

A general purpose device, the ac- and dc-specified AD7893 is suitable for both industrial measurement and DSP applications. Its small package and high level of integration permit dense circuit layouts. Its high throughput rate, low power, and single 5-V-supply operation make for a



no-fuss design in a broad spectrum of applications.

Specifications include 70 dB min SNR and –80-dB max THD (10-kHz sine sampled at 117 kps), no missing codes over temperature (–40 to +85°C). Three signal-input-range versions are available, 0 to 2.5 V FS (AD7893-2), 0 to 5 V FS (AD7893-5) and ± 10 V FS (AD7893-10), with two performance grades (A,B) for each version. Prices start at \$10 (100s). Circle 18

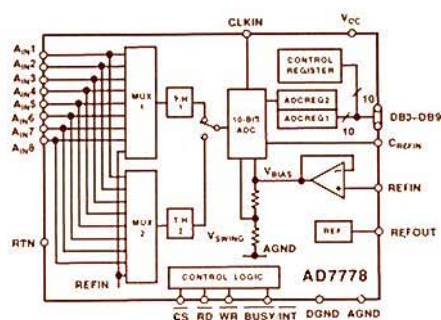
10 Bits, 400 kps, Multi-Channels

AD7776: 1, AD7777: 4, AD7778: 8 channels
Complete, No missing codes, 7.5-mW power-down

Functioning as complete single-supply, low-power data-acquisition systems, these devices form a family of 2.5- μ s-per-conversion (400 kps), 10-bit multi-channel sampling a/d converters. Each is complete, with sample-hold functions, control logic, a precision reference, and a 10-bit ADC, along with a multiplexer of appropriate width. For operation, they require only a +5-volt supply, an 8-MHz clock, and the usual decoupling capacitors. They interface directly to popular microprocessors and DSPs and offer a range of sampling options:

- AD7776: 1 channel, 24-pin SOIC
- AD7777: 4 single or 2 channels simultaneously, 28-pin DIP or SOIC
- AD7778: 8 single or any 2 channels simultaneously, 44-pin PQFP

The converters are specified with both ac and dc parameters, permitting each to be considered for both signal-processing



and measurement applications. DC specs include max integral nonlinearity of ± 1 LSB and guaranteed no-missing-codes. AC specifications include minimum $S/(N+D)$ of 57 dB and total harmonic distortion of –60 dB. Maximum power consumption is only 75 nW, dropping to 7.5 μ W in the power-down mode. Prices (1000s) are \$7.85, \$9.20, \$10.10 for the AD7776, -77, -78. Circle 17

16 Bits, 100 kps

Sigma-Delta AD776
+5-V Single Supply

The AD776 is a 100-kps, 16-bit A/D converter designed to interface analog signals to μ Ps and DSPs. Because of the high inherent $\Sigma\Delta$ sampling rate, it requires just a simple antialiasing filter and no sample-hold. It can operate from a single +5-volt supply (400-mW max dissipation), includes an on-chip voltage reference, and requires only a 1-to-12.8-MHz clock input for operation.

Its analog front end is differential, improving signal swing, PSRR and clock jitter sensitivity. Its serial output port permits easy interfacing with a variety of processors, including the Analog Devices ADSP-21xx series. Speed can be traded for resolution (400 kHz at 12 bits) using an on-chip comb filter. The AD776 is packaged in a 20-pin cerdip, with a –40 to +85°C temperature range. Price in 100s is \$18.00. Circle 18

16 Bits, 100 kps

Autocalibrated AD677
Needs no user trims

The AD677 is a general-purpose serial-output high-accuracy 16-bit sampling A/D converter packaged in a narrow 16-pin DIP. Its switched-capacitor successive-approximation architecture provides automatic calibration, resulting in a maximum integral nonlinearity spec (K and B grades) of 1.5 LSB (22 ppm). Its applications—where ac performance and dc accuracy, plus price and speed, are important—include data acquisition, signal processing, and instrumentation.

It uses ± 12 -volt (analog) and +5-volt (logic) supplies and an external 5 to 10-V reference. The K (0 to +70°C) and B (–40 to +85°C) grades have minimum SNR of 90 dB and maximum THD of 95 dB over temperature for a 1-kHz signal sampled at 83 kps. Prices (JD grade) start at \$38 in 100s. Circle 19

Single or Multiple Op Amps for Every Reason

Four on a Chip

High speed and precision OP467 saves power & room

The OP-467, with four fast op amps in one package, has the fastest slew rate (170 V/ μ s) and settling time (≤ 250 ns to 0.01%) among quads. In multichannel systems, it saves space and cost-per-channel, reduces power drain, and boosts reliability. Unity-gain stable, it can drive high-capacitance loads (≤ 1600 pF).

Besides its speed, it also offers low offset (≤ 500 μ V) and should be the first choice of designers of high-speed instrumentation and test equipment, as well as high-speed detectors, laser scanners, sonar arrays, and other applications combining speed, accuracy, and low power consumption at voltages from ± 5 to ± 15 V. It is available in 14-pin plastic DIP, cerdip, 16-lead SOL, and 20-contact LCC surface-mount packages. Its data sheet includes a SPICE macromodel. Prices (100s) start at \$6.50 (-40 to $+85^\circ\text{C}$). Circle 20

Single-Supply FET

AD820 swings rail to rail Supply range is $+3$ to ± 18 V

The AD820 is a precision, low-power FET-input op amp that can operate from a single supply from $+3$ to $+36$ V or with dual supplies from ± 1.5 to ± 18 V. Its output swings from rail to rail (within 10 mV) and its input can actually swing 0.2 V below ground. Its JFET input stage maintains low bias current (≤ 10 pA at 25°C , B grade), with offsets as low as 900 μ V max over temperature (-40 to $+85^\circ\text{C}$) and 25 nV/ $\sqrt{\text{Hz}}$ noise at 10 Hz.

Though its quiescent current drain is only 800 μ A, it will drive loads of up to 16 mA and 350 pF. It has unity-gain bandwidth of 1.8 MHz and 3 V/ μ s slew rate. A 3-volt version, AD820A-3V has specs optimized for 3-volt operation (-40 to $+85^\circ\text{C}$) at no extra cost. The AD820 is available in 8-pin plastic DIPs and SOIC. Prices start at \$1.28 in 1000s. Circle 21

1-2-4-Channels, $+5$ -V

OP113/213/413: Low drift and noise, single supply

The OP113/213/413 op-amp family are useful for amplifying low voltages in single-supply systems from $+5$ V to $+36$ V, or dual-supply systems from ± 2.5 V to ± 18 V, where low drift and voltage noise are critical requirements. Examples include precision instruments, such as digital weighing scales, also automotive sensors, strain gages and temperature transducers.

They are the lowest-noise-and-drift single-supply amplifiers [4.7 nV/ $\sqrt{\text{Hz}}$ at 1 kHz, and 0.2 μ V/ $^\circ\text{C}$, with 100- μ V offset]. In addition, their gain-bandwidth is 3.4 MHz, and they are unity-gain stable. Input common-mode range is from the negative supply rail to < 1 V of the positive rail. They are specified for 600-ohm loads on single supplies. Packages include DIPs and 8-pin SO (single and dual) SOL-16 (quad); operating temperatures are -40 to $+85^\circ\text{C}$. Prices start at \$1.60 in 100s. Circle 22

Hi-Speed, Low-Power

Dual AD826 has 50-MHz BW Drives unlimited cap loads

The AD826 chip features a pair of easy-to-use, low-power op amps for high-speed systems—combining good video and dc performance. They will work on supplies from ± 2.5 V to ± 18 V and are specified for ± 5 , ± 15 , and $+5$ -volt single-supply operation; they draw only 7.5-mA per channel. Maximum offset voltage is 2 mV (3 mV over the -40 to $+85^\circ\text{C}$ temperature range).

Dynamic performance specs include 50-MHz unity-gain bandwidth, 350-V/ μ s slew rate, and 70-ns settling time to 0.01%. For video applications, differential gain and phase are 0.07% and 0.11°. They will drive unlimited capacitive loads, deliver up to 50-mA (min), and swing a 150- Ω load ± 2 V p-p on a $+5$ -V supply.

The AD826 is available in 8-pin plastic DIPs and SOICs and is priced at \$2.10 in 1000s. Circle 23

Choose Your Gain

AD962x optimizes wideband performance at G = 1, 2, 4, 6 V/V

The AD9621, AD9622, AD9623, and AD9624 wideband op amps combine the dynamic features of current-feedback amplifiers with the simplicity and ease of use of voltage feedback. With respective minimum stable gains of $+1$, $+2$, $+4$, and $+6$ V/V and large-signal bandwidths of 130, 160, 190, and 200 MHz, harmonic distortion is -52 , -65 , -64 , and -66 dB, input noise is 80, 49, 36, and 32 μ V rms (0.1 to 200 MHz), and settling times to 0.01% are 11, 14, 14, and 14 ns.

Wide bandwidth, low distortion, fast slewing and settling, plus the ability to choose a device based on required gain, are useful in many applications. Designed for use on supply voltages from ± 3 to ± 5 V, industrial versions are available in 8-pin plastic DIP, SOIC, and cerdip; MIL versions in cerdip only. Prices for all four start at \$5.05 in 1000s. Circle 24

$+5$ -V Audio Dual

SSM-2135 can drive 25 Ω , has low noise and distortion

The SSM-2135 is a dual op amp designed for high performance in audio circuits, in such applications as headphone driver, microphone preamplifier, balanced line driver, differential line receiver, ADC and DAC buffer and filter. Its low noise (5.2 nV/ $\sqrt{\text{Hz}}$ at 1 kHz) and distortion (0.003% at 1 kHz), wide bandwidth (3.5 MHz), and versatile load-driving ability (± 30 -mA short-circuit current and only 0.005% distortion when driving a 32- Ω load) make it an excellent choice for use with codecs as a microphone preamp or output buffer in multimedia computer audio systems.

The SSM-2135 is unity-gain stable. It has a power-supply range of $+4$ to $+36$ V or ± 2 V to ± 18 V, an operating temperature range of -40 to $+85^\circ\text{C}$ and is packaged in 8-pin DIP or SOIC. Prices start at \$2.10 (100s). Circle 25

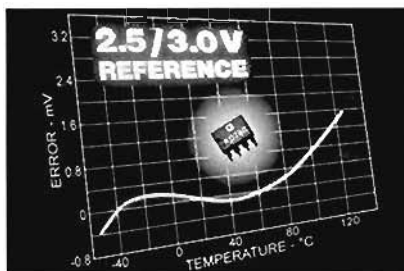
DACs, References, Color Encoder & Much More

Lo-Dropout & Hi-Accuracy References

REF-195: +5 V, can operate with a +5.10-V supply
AD780 offers 2.5/3.0 V ± 1 mV, 3 ppm/ $^{\circ}$ C

These two references provide high accuracy and excellent stability for voltages of 2.5, 3.0, and 5.0 V. Both are available at low cost in 8-pin plastic DIPs, cerdips, and SOICs, and for both, the -40 to $+85^{\circ}$ C (extended industrial) and the -55 to $+125^{\circ}$ C (military) temperature ranges.

The REF-195 is the industry's first micropower low-dropout precision reference. Its specified output is 5 volts (± 2 mV), with a 5-ppm/ $^{\circ}$ C tempco, at currents up to 30 mA; yet its quiescent current is only 45 μ A, which can be further reduced to 15 μ A in sleep mode. Its regulation against load and line is 4 ppm/mA and 4 ppm/mV, and it will work with line voltage from 15 V (to as low as 5.1 V (5.50 V min at 10 mA and 6.30 V min at 30 mA)). Prices start at \$1.94 in 1000s.



The 2.5-V AD780 can be jumpered to deliver 3.0 V, both voltages within ± 1 mV max, with a tempco of 3 ppm/ $^{\circ}$ C max. This pin-compatible upgrade of the LT1019 can source or sink 10 mA with max load regulation of 75 μ V/mA (-40 to $+85^{\circ}$ C); max line regulation of 10 μ V/V, from 4 to 36 V (≥ 4.5 V for 3.0-V output). Prices start at \$3.31 (1000s). Circle 26

Video DACs

ADV473 triple-8-b, 135 MHz
ADV7128: 1 \times 10-b, 80 MHz

The ADV473 is an improved second-source (triple-8-bit PC-speed CMOS video RAM-DAC in a 68-pin PLCC, with an on-chip voltage reference. A true-color part, it can display 16.7 million colors simultaneously; it is backward compatible with the ADV471/678 family. It is available for true-color pixel rates of 66, 85, 110, and 135 MHz and is compatible with IBM PS/2 systems, VGA/XGA, and Apple Macintosh systems. Prices (1000s) start at \$25.60 (66 MHz).

The ADV7128, a single-supply, 10-bit, CMOS DAC in a 28-pin SOIC, with data rates of 30, 50, and 80 MHz, is ideal for both video and non-video high-speed applications where space and supply voltage are limited and low dissipation (625 mW max) is required. Applications include DDS, wireless LAN, digital radio, and instrumentation. Prices start at \$4.75 (1000s). Circle 27

Dual 12-b DACPORT

Serial; single or dual supply
With amplifiers & reference

The AD7249, a 2-channel 12-bit DACPORT[®] with a serial interface, can operate from a 12-to-15-volt single supply. Complete with input shift-register, pair of 12-bit voltage-output DACs, and on-chip 5-volt reference, it provides a dual version of the AD7243 or a serial version of the AD7237/7247, for applications in measurement, control, & communications.

Each channel has three selectable output ranges, 0 to +5 V, 0 to +10 V, and ± 5 V. On a 12-volt supply, the AD7249 draws 15 mA max, or 180 mW. Max settling time is 10 μ s for a full-scale step. Two performance grades are available for the -40 to $+85^{\circ}$ C temperature range; and a -55 to $+125^{\circ}$ C grade is also available. The serial input allows for a small package size—16-lead plastic DIP and SOIC for the industrial range, cerdip for the military range. Prices start at \$14.00 in 100s. Circle 28

RGB-to-NTSC/PAL

Fully integrated encoder
No filters or delays required

The AD720 is industry's first analog RGB-to-NTSC/PAL encoder to provide video system designers with a high-performance, fully calibrated single-IC solution; no discrete low-pass filters or delay lines are required. With differential gain and phase of 0.1% and 0.1 $^{\circ}$, the composite video outputs are capable of generating "smear-free" reverse type (as small as 9-point) in applications such as PC video add-in cards, CATV converter boxes, multimedia systems, and other video imaging systems.

It provides dc-coupled and filtered luminance, chrominance, and composite voltage outputs, and can drive 75- Ω reverse-terminated loads. With ± 5 -V supplies, the AD720 dissipates 200 mW and has a 50-mW power-down mode. Housed in a PLCC, it operates from 0 to $+70^{\circ}$ C. Price (1000s) begins at \$18.39. Circle 29

Coming Attractions: Vector Processor, Temp. Controller, μ P Supervisors

The next issue of *Analog Dialogue* will feature these recently announced new products of especial interest. Technical data is available now, and so are the products themselves.

•The AD2S100 AC Vector Processor is a low-cost mixed-signal IC that greatly simplifies the design of field-oriented control systems for induction motors (\$15.39 in 1000s). Circle 30

•The TMP-01 Low-Power Programmable Temperature Controller is an easy-to-use single-chip thermostat with accurate on-board temperature sensor and heating & cooling setpoint outputs (Prices start at \$2.48 in 1000s). Circle 31

•The ADM69x are improved Micro-Processor Supervisory Circuits with existing second sources. (Prices start at \$1.15 in 5000s). Circle 32

Ask The Applications Engineer—14

by James Bryant (ADI Europe)

with Herman Gelbach (The Boeing Company)

HIGH-FREQUENCY SIGNAL-CONTAMINATION

Q. I've heard that RF can make low-frequency circuits do strange things. What's that all about?

A. I was once summoned to France because an Analog Devices Voltage-Frequency Converter (VFC), the AD654, suffered from "unacceptable variation of accuracy." I had measured the offending parts in my own laboratory and found them to be stable and within specification, but when I returned them to the customer with my test jig he was unable to reproduce my results. While considering a site visit to confirm my suspicions, I discovered that the restaurant "La Cognito" in the town where our customer was located had three stars in the *Guide Michelin*, and the chef was a "Maitre Cuisinier de France"—a title not lightly bestowed. The visit to the customer became doubly necessary. Herman, who was in England to look at data offsets in a Boeing wind tunnel test, offered to come and help—he said it was the interesting technical problem (but just before he offered I saw him earnestly consulting the *Guide Michelin*).

To drive from the Analog Devices office in Newbury in the South of England to the centre of France involves six hours of driving, a six hour ferry crossing of the English Channel, and a change from the correct side to the right side of the road. Nevertheless, driving is better than flying, because one can take more rest gear (and the portable ham-radio station as well—we are both hams).

As we approached the customer's works we passed an enormous short-wave transmitting antenna, and then another, and yet another. We began to guess what might be wrong, and when we entered the laboratory I was carrying a hand-portable two-metre ham transceiver (an HT or "handy-talky") in my jacket pocket.

The AD654 was indeed behaving unstably, as the customer had claimed. The VFC's output frequency varied by an equivalent offset of tens of mV over the space of a few minutes. I quietly reached into my pocket and pressed the transmit button of my HT. The output frequency jumped by an equivalent of 150 mV, thus demonstrating the problem to be high-frequency pickup. More-formal measurements a little later showed that the local transmitters (of the French Overseas Broadcast organization) produced high-frequency (HF) field strengths within our customer's works of tens or hundreds of mV/m.

Many problems of instability in precision measurement circuitry can be traced to high-frequency interference, but unless there is a loudspeaker in the system that might unexpectedly burst into hard rock music from the nearby radio station, it is common for engineers to overlook this source of inaccuracy and blame the manufacturer of the amplifiers or data converters.

Furthermore, this case was unusual in that it took a high-powered signal to affect the AD654, which is single-ended and also relatively insensitive to RF—it is much more common to see with a differential amplifier in-amp. Both inputs of these types of amplifier have high input impedances to common;

they are therefore far more vulnerable and are affected by low-level RF, such as radiation from a personal computer (PC). (This phenomenon will be detailed in the forthcoming Analog Devices System-Design Seminar Notes, to be offered for sale as *System Application Guide* in late 1993.)

An important factor is that, in instrumentation amplifiers, common-mode rejection decreases with increasing frequency, starting to roll off at quite low frequencies—and distortion increases with frequency. Thus, not only are high-frequency common-mode signals not rejected; they are distorted, producing offsets. For some applications, where RF interference is a strong possibility, the AD830 difference amplifier (page 8) has wideband common-mode rejection and is designed for line-receiver applications; it may be a useful substitute for an instrumentation amplifier.

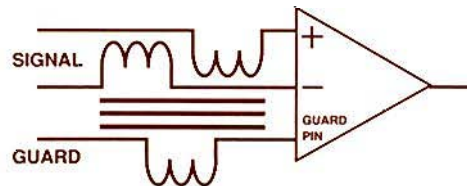
Sensors are often connected to their signal-conditioning electronics by long cables. Radio engineers have a term for such long pieces of wire; they call them *antennas*. The long feeders from sensors to their electronics will behave in the same way and will serve as antennas, even if we do not wish them to do so. It does not matter if the sensor case is grounded—at high frequencies the reactances of the case and feeders will allow the system to behave as an antenna, and any high-frequency signals (*E*-field, *M*-field, or *E-M*-field) which it encounters will appear across any impedances. The most likely place for them to end up is at the amplifier input. Precision low-frequency amplifiers can rarely cope with large HF signals, and the result is error—commonly a varying offset error.

Q. But this couldn't happen to me!

A. Never believe it won't happen to you! An easy free lunch can always be obtained by persuading an innocent to bet on his or her circuit being free of such problems. Using a ham radio HT on the two-metre (144-148-MHz) band, one wait at a distance of one meter for one second will win you your free lunch almost every time. But a less-dramatic test can be equally convincing.

Disconnect the sensor and its leads. Short-circuit the amplifier input terminals to each other and to the amplifier circuit common (probably ground) with the shortest possible links and measure the amplifier output; observe its stability over a few minutes. Now remove the short-circuit, replace the sensor leads and place them in their normal operating environment. Disable the excitation and short-circuit the signal leads at the sensor end. Again measure the amplifier output, and its variation with time. Weep quietly.

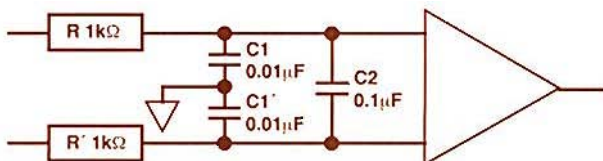
It is often possible to see what is happening by using a high-frequency oscilloscope (or a spectrum analyzer, which is more sensitive but less easy to interpret) to measure the HF noise, both normal mode and common-mode, at the amplifier input; but normal mode measurements must be treated with some suspicion, because the oscilloscope itself—and its power- and probe leads—may themselves introduce signals and invalidate the measurement. The effect of the oscilloscope may be minimized by using a simple broadband transformer between the measurement point and the oscilloscope input, as shown in the figure; but such a transformer has fairly low impedance and will load the circuit being measured.



Common-mode signals can be observed quite easily by disabling any sensor excitation and connecting the oscilloscope ground to the ground at the board input and joining all the sensor leads together and to the oscilloscope input. All too often this signal will have an amplitude of several hundred millivolts and contain components from low frequencies to tens or hundreds of MHz.

The world is full of HF noise sources: ham radio operators, police, people with portable phones, garage door openers, the sun, supernovas, switching power-supply and logic signals (e.g., PCs). Since we cannot eliminate HF noise in the environment, we must filter it out of low-frequency signals before they arrive at precision amplifiers.

The simplest type of protection can be used when the signal bandwidth is only a few Hz. A simple RC low-pass filter inserted ahead of an amplifier will afford both normal-mode and common-mode HF protection. A suitable circuit is shown in the figure. There are two important issues to be considered in the choice of components: the resistances R and R' (shown as $1\text{ k}\Omega$ in the diagram, a value suitable for amplifier bias currents of a few nA or less) must be chosen so that they do not increase the offset appreciably as the amplifier bias current flows in them. The normal-mode time constant, $(R + R')C_2$, must be much larger than the common-mode time constants, RC_1 and $R'C_1'$, otherwise the common-mode time constants would have to be very carefully matched to avoid an imbalance that would convert the common-mode to a signal between the differential inputs.



If the signal bandwidth is wider, such simple filters will not be suitable because they remove the desired HF normal-mode signals as well as the unwanted HF common-mode signals. Large HF common-mode signals are very likely to suffer common-mode—normal mode conversion (as well as minor rectification, producing low-frequency errors) if they get to the amplifier, so it is necessary to use a filter which will reject HF common-mode signals but will pass DC and HF normal-mode signals.

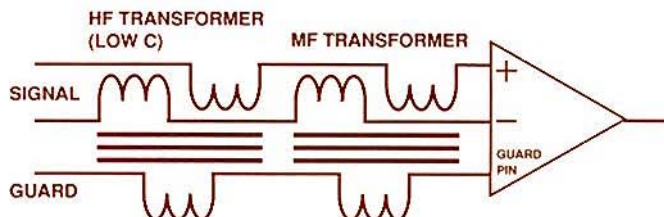
Such a filter is shown below. It was devised many years ago by Bill Gunning of Astrodats and is related to the “phantom circuit” used in long-distance telephone circuits. It uses a tightly coupled “trifilar” transformer having three windings in an accurate 1:1:1 ratio. An AC voltage across any winding will also be present on the others.

The guard line is connected to ground at the source end and at the other end to the amplifier’s guard pin (or a comparable

derived voltage), which represents what the amplifier “thinks” is common mode, via a capacitor. The high-frequency common-mode signal will appear (by definition) across the bottom winding, and will induce an equal common-mode voltage in the other two, subtracting the common-mode voltage in series with each line and effectively cancelling the HF common-mode signal at the amplifier inputs.

There are, of course, potential problems. A capacitor in series with the transformer is almost essential in the guard circuit to block DC and LF and prevent transformer core saturation by low-frequency currents in the guard circuit. The impedance looking into the amplifier guard terminal must be much lower than the impedance of the transformer windings; and at very high frequencies the capacitances of the transformer will allow signal leakage or may cause phase shift. These issues set incompatible constraints on the design of the transformer, if it must deal with a very wide range of common-mode frequencies.

In such a case double cancellation using two separate transformers as shown might be considered—the one nearer the amplifier having high inductance (and correspondingly high capacitance) and the other having good VHF efficiency.



Other approaches are also possible: the amplifier can be sited closer to the sensor and the long leads be replaced by leads (or optical fibre) carrying digital data, which is less vulnerable; more shielding is often (but not always) helpful; and sometimes (but rarely) it is possible to reduce the possibility of unexpected HF signals (even if you keep away the hams and police, there is always the possibility of the unexpected pizza delivery truck radioing to its base . . .)

The most important consideration, though, is awareness of the possibility of HF interference and readiness to tackle it. If designs are always made in the expectation of unwanted HF, chances are excellent that precautions will be adequate—it’s when you don’t expect it that the trouble starts.

- Q. How did it work out with the French customer?
- A. His problem was cured with two resistors, three capacitors and a piece of grounded copper foil. We went off to “La Cognette” to celebrate. ▶

Use Analog I/O Ports as High-Performance Infinite Sample/Holds and Peak Followers

by Mike Curtin and Albert O'Grady

The challenges in acquiring signals rapidly and accurately with high-speed sample-and-hold amplifiers are well known and documented. However, less well-known is the problem at the other end of the spectrum: finding a sample-and-hold that will retain the held signal for a significantly long time without losing accuracy due to droop.

The essential memory element in an analog sample-and-hold amplifier is the hold capacitor. There is a trade-off between capacitance, acquisition time, and droop rate. To get a fast acquisition time, the hold capacitance should be low, but to get a low droop rate the capacitance should be high. Normally, a compromise is reached, depending on the application. A typical specification for droop rate is 0.1 V/s (often specified as 100 mV/s or even 100 μ V/ms). If it is required to hold the signal for 10 ms, for example, there will be a 1-mV error voltage due to the droop rate. This is often significant in peak-detectors and in sample-and-hold applications which need long hold times. The option of increasing the hold capacitance has its drawbacks, as acquisition time and aperture time will be increased as a result.

A definitive solution to the problem is the concept of the infinite sample-and-hold. This consists of digitizing the input signal at or near the desired point in time (sampling instant) with a fast sampling ADC, and using a D/A converter to reconstruct and hold the signal until a new sample is required. With the advent of increased integration in converter circuits, this solution is increasingly practical. It can be implemented ever more economically, occupying less board area and using less power. Figure 1 shows a single device capable of embodying both functions.

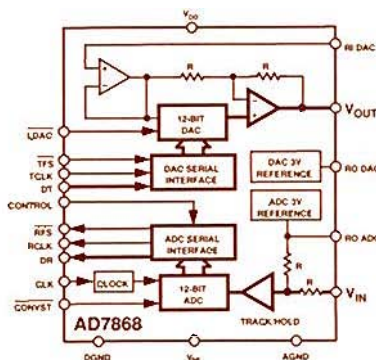


Figure 1. 12-bit sampling A/D and D/A on a chip.

The throughput of a conventional sample-and-hold amplifier is limited by acquisition time and aperture time. This is critical in high-speed applications. However, in fast-acquisition, long-hold

applications, the delay between the hold command and the output switching to a new value is not as critical. The droop rate becomes the critical performance specification, since hold error increases with time. Figure 2 shows a typical implementation of an infinite sample-and-hold amplifier, using a sampling A/D and a D/A on a single monolithic chip. For very high performance, separate converters could be used, but this solution, employing commonly available devices, such as the AD7868 or AD7869*, results in a compact, self-contained solution. In addition, the use of a common on-chip reference for both converters can result in superior tracking between analog input and analog output.

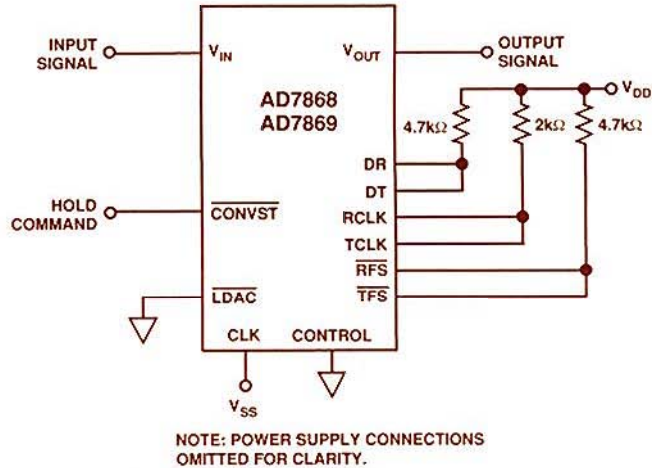


Figure 2. Sample/infinite-hold circuit using AD7868 or AD7869 monolithic analog input/output ports.

Figure 3 shows the timing diagram. When the Hold command is given, the ADC section begins conversion and the serial data stream comes out on DR. At the same time it is clocked into the D/A section through the DT pin. At the end of conversion, the D/A converter output automatically updates to the new value.

The D/A converter settling-time spec determines the time to reach the final held value. Once this value has been reached, the output is held until the next Hold command is applied. Either 12- or 14-bit accuracy can be achieved depending on the device used.

12-bit system: AD7868

$$\text{Hold Delay Time} = 10 \mu\text{s (conversion time)} + 3 \mu\text{s (D/A Settling Time)} = 13 \mu\text{s}$$

14-bit system: AD7869

$$\text{Hold Delay Time} = 10 \mu\text{s (conversion time)} + 4 \mu\text{s (D/A Settling Time)} = 14 \mu\text{s}$$

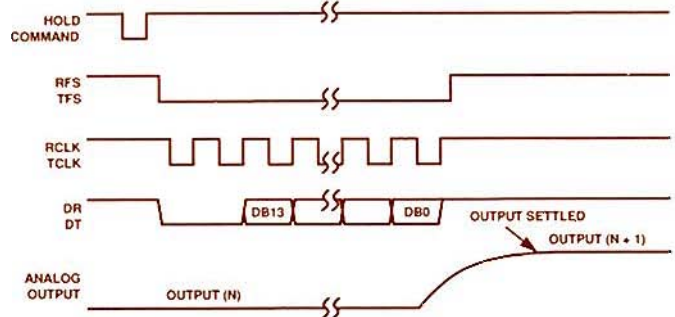


Figure 3. Timing Diagram.

*Use the reply card for technical data. Circle 33

The 4-to-20-mA current flowing in the loop is usually converted to voltage for further signal processing, or conversion to digital, by means of a high-wattage 250-Ω resistor, for an input voltage range of 1 to 5 V. When this voltage is applied directly to a conventional converter with a 0-to-5-volt range, 20% of the converter's range is wasted. In addition, after conversion, the converted digital signal must be re-interpreted with the offset subtracted out, and some form of calibration must be used to trim any errors in offset or scale-factor in the original input signal.

The AD7712 has a system calibration function which allows the user to apply the zero-scale and full-scale input voltages during a calibration cycle. The full span of the ADC will be adjusted to extend from the zero-scale voltage to the full-scale voltage. The range of calibration is from 80% to 105% of the nominal input span. With a gain of 2 and unipolar input range selected for AIN2, the nominal input span is interpreted as 0 to 5 V. The allowable range for system calibration is thus from 4 V (80% of nominal) to 5.25 V (105% of nominal). Therefore, the AD7712 can apply system calibration utilize the full range of the ADC to represent the 1-to-5-volt range applied to the input terminals.

The zero-scale of the input span is calibrated by applying the input voltage corresponding to 4 mA of current flowing in the loop and performing the first calibration step (offset), interpreting whatever that voltage is as zero-scale. Then full-scale is calibrated by applying the input voltage corresponding to 20-mA in the loop, and performing the second calibration step (full-scale), to interpret that level as full-scale. As a result, the AD7712 will output all 0s when 4 mA is flowing in the loop, and all 1s when 20 mA flows in the loop. The drop across a small additional series resistance can be monitored by AIN1 to detect the absence of loop current in open-circuit fault conditions.

For applications where 0 mA flowing in the loop needs to be recognized (including loops for which the full-scale measurement range is 0 to 20 mA), calibration coefficients can be written to the AD7712's calibration registers to accept a 20-mA input span. ▣

DIGITIZE STRAIN-GAGE BRIDGE DIRECTLY

Figure 6 shows an AD7710 providing excitation for, and differential readout from, a strain-gage bridge. The AD7710 is ideal for such applications. The software-programmable gain provides a range of sensitivities to below 20 mV full-scale. Common-mode rejection is better than 92 dB from dc to several kHz, and on-chip digital filtering extends it to 150 dB at line frequency and its multiples.

The bridge network shown has two active gages and balancing resistors equal to the unloaded resistance of the gages. Their resistance increases as they are loaded, to typically about 1.02 to 1.04 of their rest value. Current excitation, I_E , is provided by the AD707, connected as a current source. The constant voltage at REF OUT must be duplicated at the feedback terminal, "A", forcing the AD707 to supply a constant current equal to V_{REF}/R_E to flow through R_E and the bridge.

As the bridge is loaded and the gage resistances increase, a differential voltage is developed across the bridge output:

$$V_O \approx I \times \Delta R/2$$

R_E determines the excitation current, which determines the bridge's sensitivity, and the maximum ΔR establishes the full-scale input to the AD7710. Assuming 350 Ω as the nominal bridge resistance, 4% as full-scale variation (14 Ω), and 20 mV as the corresponding output voltage to the AD7710, the bridge current should be about 2.85 mA. With a 2.5-V reference, the required value of R_E would about 877 Ω. However, because of the substantial calibration range of the AD7710, a standard 1-kΩ resistor could be used (17.5 mV).

The circuit has the additional benefit that if REF OUT varies (with temperature or from device to device), I_E varies proportionally, as does the bridge output. Therefore, a fixed output code will result from a given value of strain, regardless of REF OUT's variation. The calibration features of the AD7710 are helpful in reducing drift effects in the device or R_E . With simple additional circuitry, the effects of tare in weighing mechanisms can be corrected for. ▣

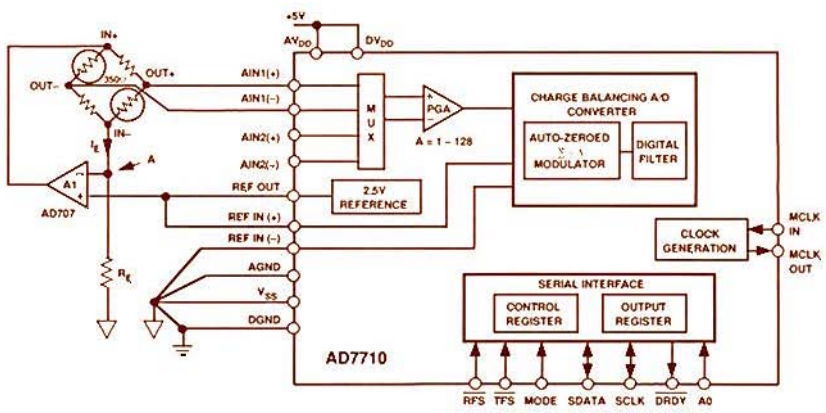


Figure 6. Strain-gage solution using the AD7710.

*Use the reply card for technical data on the AD771x family. Circle 34

Analog Devices Names Three New Fellows

Three new Fellows were introduced at the Analog Devices 1993 General Technical Conference: Mohammad Nasser, Brad Scharf, and Jim Wilson.

Fellow, at Analog Devices, represents the highest level of advancement that a technical contributor can achieve, on a par with Vice President. The criteria for promotion to Fellow are very demanding. Fellows will have earned universal respect and recognition from the technical community for unusual talent and identifiable innovation at the state of the art; their significant technical contributions will have had a major impact on the company's revenues; they must have demonstrated superior creative ability in product- or process technology leading to commercial success.

Other attributes include roles as mentor, consultant, organizational bridge, gatekeeper, entrepreneur, teacher, and ambassador. They must also be effective as leaders of teams and contributors to team effort and in understanding the voice and needs of the customer. Our three new Fellows' accomplishments and technical abilities, as well as their personal qualities, make them well-qualified for this appointment. They join Fellows Derek Bowers (1991), Paul Brokaw (1980), Lew Counts (1984), Barrie Gilbert (1980), Jody Lapham (1988), Fred Mapplebeck (1989), Jack Memishian (1980), Wyn Palmer (1991), Carl Roberts (1992), Mike Timko (1982), Bob Tsang (1988), and Mike Tuthill (1988).

MOHAMMAD NASSER

Mohammad joined Precision Monolithics, Inc. (which became ADI's PMI Division) in 1980. During the early '80's he was the key engineering contributor to developing PMI's CMOS technology and led the development of PMI's proprietary thin-film process. He is also responsible for the family of complementary-bipolar-CMOS (CBCMOS) processes, including a process with a patented buried-layer structure that requires a greatly reduced number of mask levels. These processes have been responsible for major contributions to the product mix and revenues of PMI.

Mohammad is unique among fab people in that he designs circuits himself; there is perhaps no better way to understand the needs of the circuit designers who are the clients of process development than to be a designer oneself. He also integrates process development with manufacturing discipline right from the start—in fact they are inseparable; Mohammad does both.

He earned an MS in solid-state physics at UCLA and continued his studies toward a Ph.D. degree. He has since made essentially his entire career with PMI and Analog Devices. He has lived in the U.S. for 20 years and in northern California since 1980. Mohammad and his wife, Diane, married 14 years, have two young sons. His major external interest is spending time with his family and taking care of his pool and backyard. He is an enthusiastic investor and works on his portfolio using his PC. He loves to play all card games and enjoys travel to places such as Europe and Las Vegas, for both business and pleasure.

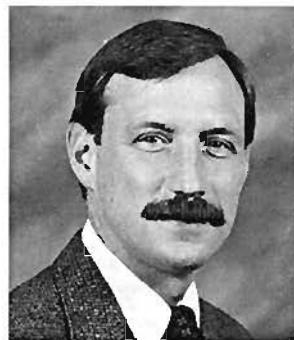


BRAD SCHARF

Brad joined Analog Devices in 1981 and, in his first assignment, working with (1988 Fellow) Jody Lapham, won a joint patent covering the use of p-epi for complementary bipolar processes. He later worked on the FLASH process, essential to a number of highly successful products. In the mid-eighties, Brad began experimenting with polysilicon emitters, and this work eventually led to several generations of ABCMOS, which is key to high-speed mixed-signal products. His recent studies in modern submicron bipolar technology will be important to processes for future generations of mixed-signal products.

Besides his technical accomplishments and commercial successes, Brad has demonstrated the softer qualities of technical leadership. He is known for developing processes that are robust in manufacturing, and for concentrating on manufacturability even during the early stages of development. He is an advocate of customer focus as an important element of process-development strategy.

Brad earned his bachelor's degree (BSEE) at Southern Methodist University, in Dallas, and earned both his Master's and Ph.D. degrees at Stanford. While at Stanford, he enjoyed camping, backpacking and hiking. After graduation, Brad spent 2 1/2 years working in Germany and touring Europe, Egypt, and Israel. His wife, Mary White-Scharf, is an immunologist department manager at a biotech startup company. They have two sons and a daughter. Brad enjoys participating and watching all sports—especially during the playoff season. He plays basketball, baseball, volleyball, and casual football—and the guitar—with enthusiasm.



JIM WILSON

Jim began his career at Analog Devices 15 years ago as a test-engineering manager at Analog Devices, BV, in Limerick, Ireland. Here, he gained valuable understanding of what it takes to get new products into profitable, high-volume production. He also gained experience as a Senior Applications Engineer, refining his skills in interpreting customer's requirements and translating them into solutions.

In 1980, he joined the embryonic DSP division, and for the last 12 years has led the design of floating-point building-block products and mixed-signal products, which have been responsible for substantial revenues. Jim has recently been working with the audio codec group to develop such products as the recently announced—and already highly successful—AD1848 and 1849.

Jim was born in Northern Ireland and educated in Scotland. He has two sons. His hobbies include chess, golf, and reading. His interests are in anything involving math and digital signal-processing.



Worth Reading

NEW BOOK

Applications Reference Manual, 1,344 pages, softcover, 1993, published by Analog Devices, \$9.95. A compilation of the "best" of technical articles from the trade press, application notes, *Analog Dialogue* articles, and design tutorials by Analog Devices authors. Arranged by device or application classification, and cross-indexed by model number, subject, application-note number, and author. Includes conversion charts in an Appendix. Use the book order card, fax or phone the Literature Center.

SPICE MODEL LIBRARY disk, release H (7/93). 352 macromodels, including 34 new models, and featuring the first-ever CMOS-switch macromodel. Circle 35

BROCHURES AND GUIDES

High-Speed Op Amp Selection Guide, 1993 update. A 6-page short-form highlighting new products. Circle 36

Personal Sound Architecture—a programmable architecture for flexibly integrating sound into personal computer systems. Circle 37

Corporate Capabilities Brochure, "Leadership in Real-World Signal Processing." Some answers to the question: What is Analog Devices? Circle 38

SERIALS

DSPatch—The DSP Applications Newsletter: Number 26, Winter, 1993 (16 pages): Features Compression Labs' Cameo Personal Video™ system; the ADSP-2115; C compiler for the ADSP-21000 floating-point family, based on the Free Software Foundation's GNU compiler. Also includes: Formant speech analysis, DSP-augmented ham radio, SCELSP speech coding, ADSP-2105 booting from host, ADA compiler for ADSP-21020. Circle 39

Number 27, Spring, 1993 (20 pages): Features ICASSP '93, Signal Computing Technical Exchange, and introduction of the ADSP-2103. Also features CSDK-100 Compressed Speech Design Kit. Also includes: C programming for DSP; New 3rd-party development tools, and new software releases for ADSP-2100 and 21000 families. Circle 40

Analog Briefings—The Newsletter for the Defense/Aerospace Industry. Vol. 9, no. 1 (6 pages + ADC information card). Features high-speed A/D conversion, Testing op amps, Multichip modules, New products. Circle 41

APPLICATION NOTES

Using the AD2S80A Series Resolver-to-Digital Converters as a control transformer, by John Christacopoulos (AN-203). Circle 42

Bootstrapped IC substrate lowers distortion in JFET op amps, by Walt Jung (AN-232). Circle 43

Evaluation Board for the AD7710, 24-bit sigma-delta A/D converter, by Mike Byrne and Albert O'Grady (AN-241). Circle 44

A low-noise microphone preamp with a phantom power option, by Walt Jung and Adolfo Garcia (AN-242). Circle 45

Circuit delivers 16-bit, 150-kHz multichannel sampling system, by Mike Curtin, Albert O'Grady, and Sean O'Leary (AN-341). Circle 46

Enhancing the performance of the AD7111A and AD7112 LOGDACs®, by Albert O'Grady (AN-364). Circle 47

Evaluation Board for the AD7712, 24-bit sigma-delta A/D converter—a signal-conditioning ADC, by Mike Byrne and Albert O'Grady (AN-365). Circle 48

Evaluation Board for the AD7711, 24-bit sigma-delta A/D converter—a signal-conditioning ADC with RTD excitation, by Mike Byrne and Albert O'Grady (AN-366). Circle 49

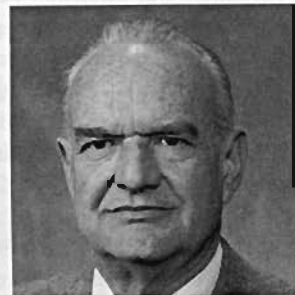
Evaluation Board for the AD7713, 24-bit sigma-delta A/D converter—a loop-powered signal-conditioning ADC, by Mike Byrne and Albert O'Grady (AN-367). Circle 50

Thermocouple signal conditioning using the AD594/AD595, by Joe Marcin (AN-369). Circle 51

MORE AUTHORS (continued from page 2)

James Bryant (page 28) is European Applications Manager for ADI, based in Walton-on-Thames, England. His photo and a biographical sketch appeared in *Analog Dialogue* 26-2.

Herman Gelbach (page 28) is a Principal Engineer at the Boeing Company in Seattle, Washington. He has been involved in aerodynamics instrumentation for some 40 years and authored several papers on related topics, most recently one on high-frequency induced errors in data-system amplifiers. He holds a BSEE from Washington State University, is a Registered Professional Engineer, and has held an amateur radio license (W7JPU) since 1942. His outside interests involve the outdoors, including rockhounding and fishing.



Mike Byrne (page 30) is a Staff Engineer with the Applications Group in Limerick, Ireland, where he provides customer support and is involved with new-product definition for CMOS converter products. He holds a B.Sc. in electronic systems from the University of Limerick. A patent-holder, he is the author of several application notes and technical articles. His leisure-time activities include music and outdoor sports.



Albert O'Grady (page 30) is a member of the Applications Group at Analog Devices BV, Limerick, Ireland in support of both analog-to-digital and digital-to-analog converter products. He holds a B.Eng. from the University of Limerick. In his spare time, Albert enjoys reading and plays badminton and tennis.



Mike Curtin (page 30) is a Senior Applications Engineer at our Limerick, Ireland, facility. His photo and a biographical sketch appeared in *Analog Dialogue* 27-1.

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

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- **8-bit, 20-MHz, 60-mW single-supply sampling ADC** with existing 2nd sources. Request **AD775** or **circle 58**
- **Precision quad 3-V op amp with rail-to-rail output**, low offset, low power. Ask for **OP-495** or **circle 59**
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- Complete serial/byte-input **16-bit DACPORT®** in 24-pin skinny DIP and SOIC. Ask for **AD660** or **circle 61**
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STOP PRESS—NEW LITERATURE:

- **Short-form designers' guide**, 160-page guide to the Analog Devices product line. Includes selection trees, selection guides, comprehensive index to all products, new-product information, and a product package listing. **Circle 68**

ERRATA & CHANGES • • • **OP-295** data sheet, rev. 0, Page 9, Figure 5: "5" in the gain formula should be "6". Also, delete the last sentence on page 8, relating to that circuit's common-mode range. • • • **AD1849** data sheet, rev. 0: an interim errata sheet is available until rev.1 (which includes **AD1849K**) is published • • • **AD2S83** data sheet, page 2, under **VELOCITY SIGNAL**, Linearity spec is changed to ±0.15% typical, ±0.25% max for 0-500 kHz, and ±0.25% typical, ±1.0% max for 0.5-1 MHz; Reversion Error is ±0.5% typical, ±1.0% max. The original specification is available with a special part number • • • **AD396** data sheet, page 2, and also 1992 Data Converter Reference Manual, Vol. 1, page 2-40, under **REFERENCE INPUTS**, Input resistance spec is 2.9 kΩ min, 6.6 kΩ max.

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PATENTS • • • 5,184,130 to Christopher Mangelsdorf for **Multi-stage A/D Converter** • • • 5,192,922 to Edward Jordan for **Anti-false triggering system for a pulsewidth modulation system** • • • 5,195,827 to Jonathan Audy and Barrie Gilbert for a **Multiple sequential excitation temperature sensing method and apparatus** • • • 5,198,785 to Edward Jordan for **Dual edge pulse width modulation system** • • • 5,208,559 to Edward Jordan for **Pulse shaping system for a pulse width modulation system** • • • 5,210,537 to Christopher Mangelsdorf for a **Multi-stage A/D converter** • • • 5,220,206 to Stephen Tsang and Gregory Koker for **Control apparatus with improved recovery from power reduction and storage device therefor** • • • 5,225,811 to Jonathan Audy for **Temperature limit circuit with dual hysteresis** • • • 5,227,670 to Paul Brokaw for **Electronic switch with very low dynamic "on" resistance utilizing an op amp** • • • 5,237,209 to Robert Brewer for **Bipolar voltage doubler circuit**.

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IN THE LAST ISSUE

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For a copy, circle 52.

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